Instruction Manual

Tektronix

DAS 92DM911
Futurebus+ Bus Support

070–8747–00

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to the Safety Summary prior to performing service.

Please check for change information at the rear of this manual.

First Printing: February 1993

Instrument Serial Numbers

Each instrument manufactured by Tektronix has a serial number on a panel insert or tag, or stamped on the chassis. The first letter in the serial number designates the country of manufacture. The last five digits of the serial number are assigned sequentially and are unique to each instrument. Those manufactured in the United States have six unique digits. The country of manufacture is identified as follows:

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Preface: GUIDE TO DAS 9200 DOCUMENTATION

The Digital Analysis System (DAS) 9200 documentation package provides the information necessary to install, operate, maintain, and service the DAS 9200. The DAS 9200 documentation consists of the following:

- a series of microprocessor-specific **microprocessor support instructions** that describe the various microprocessor support packages.
- a **system user manual** that includes a beginning user's orientation, a discussion of DAS 9200 system-level operation, and reference information such as installation procedures, specifications, error messages, and a complete system glossary.
- a series of **module user manuals** that describe each of the DAS 9200 acquisition, pattern generation, and optional I/O modules.
- an **on-line documentation** package that includes context-sensitive technical notes.
- a **programmatic command language user manual** that describes the set of programmatic commands available for remotely controlling the DAS 9200.
- a series of **application software user manuals** that describe the various application software packages.
- a **technician's reference manual** that helps a qualified technician isolate DAS 9200 problems to the individual module level and determine corrective action (including on-site removal and replacement of modules).
- a **verification and adjustment procedures manual** that allows a qualified technician to make necessary adjustments and verify specifications of the mainframe and modules.
- a series of **workbooks** that teach concepts about the DAS 9200 acquisition modules and pattern generation modules.

GENERAL SAFETY SUMMARY/ DISASSEMBLERS

The general safety information in this summary is for operating and servicing personnel. Specific warnings and cautions can be found throughout the manual where they apply and may not appear in this summary. While using this product you may need to access parts of the DAS 9200 mainframe system; if so, read the General Safety Summary in your *DAS 9200 System User Manual* for warnings and cautions related to operating the mainframe system.

TERMS IN THIS MANUAL

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

TERMS AS MARKED ON EQUIPMENT

CAUTION

CAUTION indicates a hazard to property, including the equipment itself, and could cause minor personal injury.

WARNING

WARNING indicates solely a personal injury hazard not immediately accessible as you read the marking.

DANGER indicates a personal injury hazard immediately accessible as you read the marking.

SYMBOLS AS MARKED ON EQUIPMENT

DANGER High Voltage	Protective ground (earth) terminal	ATTENTION Refer to manual

USE CARE WITH COVERS REMOVED

To avoid personal injury, remove jewelry such as rings, watches, and other metallic objects before removing the cover. Do not touch exposed connections and components within the product while the power cord is connected.

REMOVE FROM OPERATION

If you have reason to believe that the instrument has suffered a component failure, do not operate the instrument until the cause of the failure has been determined and corrected.

USE THE PROPER FUSE

To avoid fire hazard, use only a fuse of the correct type, voltage rating, and current rating.

REMOVE LOOSE OBJECTS

During disassembly or installation procedures, screws or other small objects may fall to the bottom of the mainframe. To avoid shorting out the power supply, do not power on the instrument until such objects have been removed.

DO NOT OPERATE IN EXPLOSIVE ATMOSPHERES

To avoid explosion, do not operate this product in an explosive atmosphere unless it has been specifically certified for such operation.

Section 1: OVERVIEW

This section provides basic information on the following:

- the 92DM911 Bus Support product
- software compatibility
- DAS 9200 configuration
- this manual

The 92DM911 Bus Support product disassembles data from systems that are based on the 12SU Hard Metric IEEE 896 Profiles A, B, and F Futurebus+ bus. The 92DM911 product runs on a DAS 9200 logic analyzer equipped with one, two, or three 92A96 Acquisition Modules.

The Futurebus+ bus is actually two buses: the Arbitrated Messages bus, and the Main bus. The 92DM911 product supports compelled transactions on a 32-, 64-, or 128-bit wide Main bus. The 92DM911 product does not acquire or display data for packet data beats.

The 92DM911 product acquires, disassembles, and displays data in the Disassembly display for the Main bus only. You can also display Main bus data in the State and Timing displays.

The product also acquires state data for the Arbitrated Messages bus. You can display acquired data from the Arbitrated Messages bus in the State or Timing displays.

Table 1-1 shows the number of 92A96 Modules you can have in your DAS 9200 system and the Futurebus+ buses they can support.

Table 1-1
Product Support

No. of Modules	Supported Futurebus+ Buses
1	Lower 32- or 64-bits of the Main bus only* or Arbitrated Messages bus only
2	32-, 64-, or 128-bits of the Main bus only or Lower 32- or 64-bits of the Main bus* and Arbitrated Messages bus
3	32-, 64-, or 128-bits of the Main bus and Arbitrated Messages bus
*Asynchronous control signals not available.	

This product consists of software on a floppy disk, a probe adapter, and this manual. The software includes setup files, a demonstration reference memory, symbol tables, and a disassembler program. A complete list of accessories and options is provided at the end of *Appendix C: Service Information.*

A demonstration reference memory is provided so you can see an example of disassembled bus mnemonics. You can view the reference memory without connecting the DAS 9200 to your system under test. The reference memory is automatically installed on the DAS 9200 when you install the disassembler software. Directions for viewing this file are in *Section 4: Acquiring and Viewing Disassembled Data*.

To use this product efficiently, you need to have the following:

- knowledge of your Futurebus+ system
- knowledge of your DAS 9200 configuration and its operation
- this manual
- the *DAS 9200 System User Manual*
- the *92A96 Module User Manual*, Tektronix, Inc. 1992

DAS 9200 SYSTEM SOFTWARE COMPATIBILITY

The 92DM911 Bus Support Product is compatible with the DAS 9200 System Software Release 2, Version 1.51 or higher, and DAS 92XTerm System Software Release 3, Version 1.2 or higher.

DAS 9200 CONFIGURATION

To use the bus support product, your DAS 9200 must be equipped with at least one 92A96 Module and four standard data acquisition probes.

Figure 1-1 shows an overview of the DAS 9200 connected to a typical probe adapter.

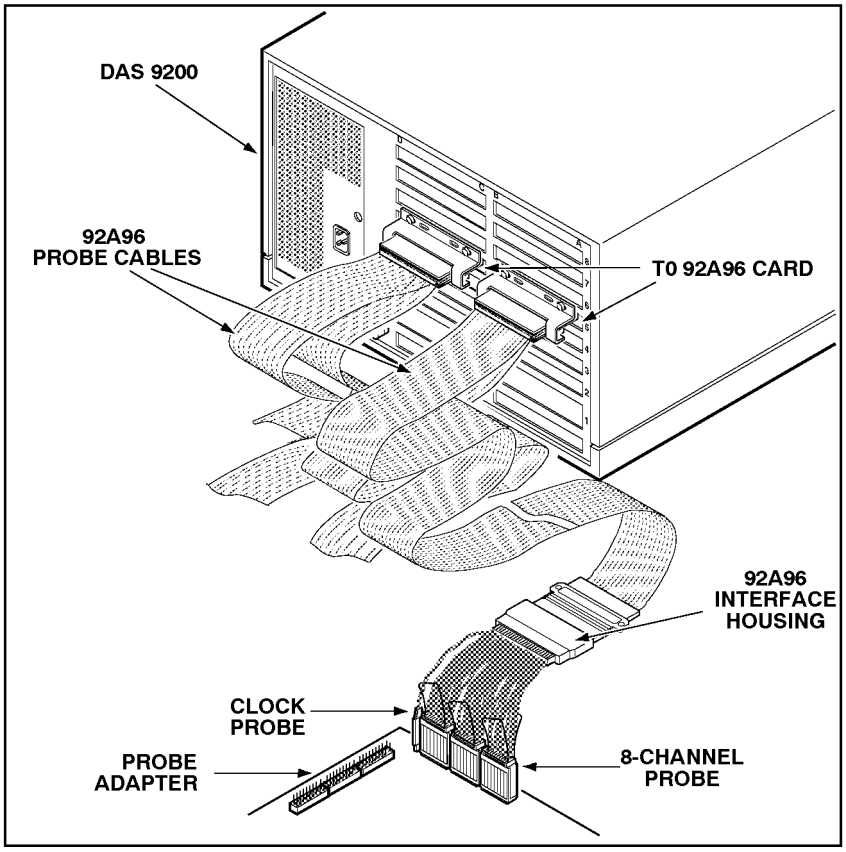


Figure 1-1. DAS 9200 connected to a typical probe adapter.

ABOUT THIS MANUAL

This manual is based on the assumption that you are familiar with the operation of the DAS 9200 mainframe and the 92A96 Acquisition Module. Therefore, details about system software and how to move through the menu structure are not provided. An overview of those functions is provided so that you do not need to consult another manual.

This manual provides detailed information on how to do the following:

- connect to your system under test
- setup disassembler software and use it
- view acquired data
- maintain disassembler hardware

Read *Section 5: General Purpose Analysis* if you are going to acquire and view timing or state data for purposes other than disassembly.

Manual Conventions

The following conventions are used in this manual:

- the term Arb bus refers to the Futurebus+ Arbitrated Messages bus signals.
- the term Main bus refers to the remaining Futurebus+ bus signals.
- the terms disassembler and disassembler software are used interchangeably in reference to the 92DM911 software that disassembles bus cycles into mnemonics and transaction types.
- the term system under test (SUT) is used to refer to the bus system from which data is being acquired.
- references to 92A96 Modules include all versions of those Modules unless otherwise noted.

Section 2: INSTALLATION AND CONNECTIONS

This section describes how to do the following:

- configure the DAS 9200
- position the 92A96 Modules in the DAS 9200
- install the disassembler software
- connect the DAS 9200 to the system under test (SUT)
- configure the probe adapter

CONFIGURING THE DAS 9200

To acquire data from a 128-bit wide Main bus, two 92A96 Modules are required. They must be configured into one variable-width module.

When using a variable-width module, both 92A96 Modules must be positioned in adjacent DAS 9200 slots. The module in the higher-numbered slot is referred to as the HI module; the module in the lower-numbered slot is referred to as the LO module. You cannot use slots 1 or 8 when creating a variable-width module. The modules do not need to have the same memory depth.

Probe connections on the probe adapter board are labeled to identify which module and which probe group connects to them. For example, LO_A0 indicates the A0 group from the LO Module.

If acquiring data from a 128-bit wide Main bus, you should check the System Configuration menu to verify that the variable-width module is defined correctly. Figure 2-1 shows how the Sys Config menu looks when two 92A96 Modules are combined into a variable-width module.

Refer to your module user manual for additional information about variable-width modules, connecting probe cables, and positioning and installing 92A96 Modules.

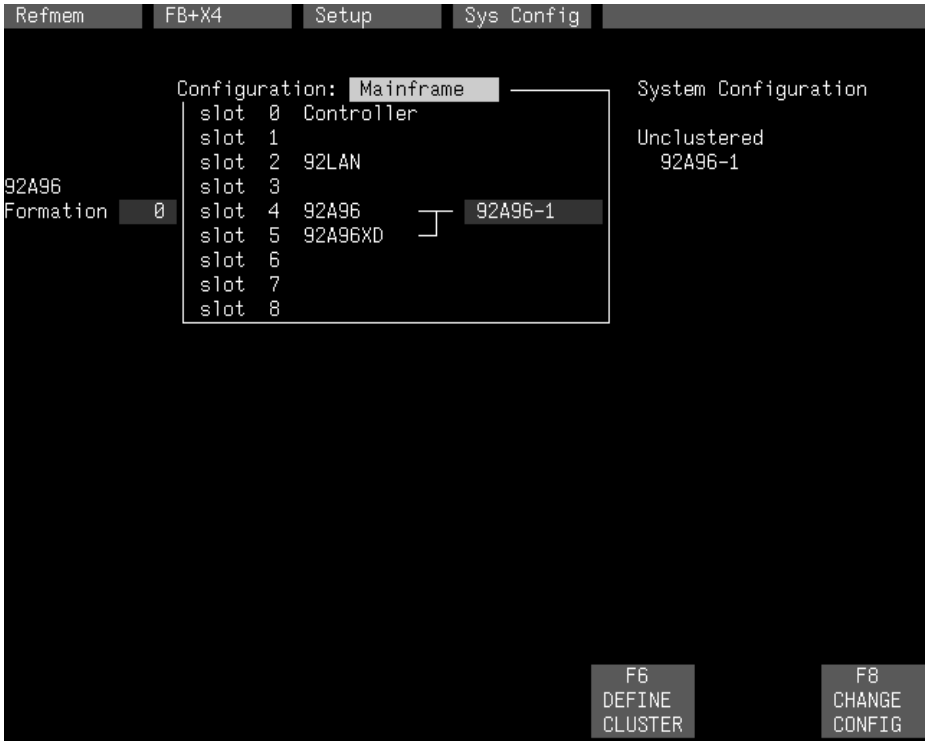


Figure 2-1. Sys Config menu with a variable-width module defined.

In a multimodule system, it is easier to identify which modules are connected to the probe adapter if slot number labels are applied to the 92A96 probe interface housings and DAS 9200 mainframe. Figure 2-2 shows how to apply slot number labels.

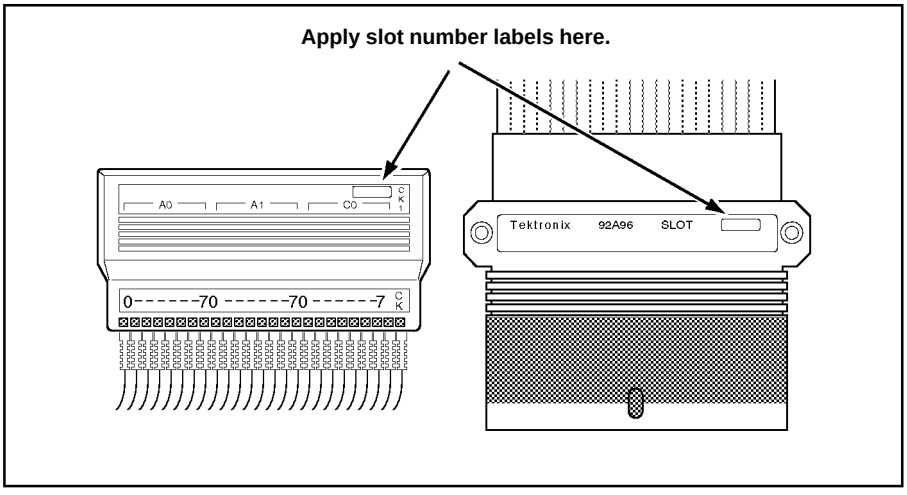


Figure 2-2. Applying slot number labels.

INSTALLING SOFTWARE

Before installing the bus application software, you should be aware that there are two different versions of DAS 9200 system software: the 9201T version and the 92XTerm version. The 9201T version allows you to operate the DAS 9200 from a 9201T terminal. The 92XTerm version allows you to operate the DAS 9200 in an X window on a workstation.

NOTE

To use the bus support package, you must install application software that is compatible with your DAS 9200 mainframe configuration and system software.

Three floppy disks are shipped with the 92DM911 bus support. To determine which floppy disk contains compatible application software, follow these steps:

1. Note the terminal type on which the DAS 9200 system software will run.
2. Power on the DAS 9200 mainframe or system, and press the Select Menu key.
3. Select the HW/SW Version menu in the Utilities column and press Return.
4. Look at the System Software line to find the version of system software loaded. Use Table 2-1 to choose the appropriate floppy disk to install.

Table 2-1
Choosing the Correct Floppy Disk

Terminal Type	System Software Line Information*	Install Floppy Disk Labelled
9200T/9201T	Release 2, Version 1.50	DAS 9200 Application Software - 92DM911
9200T/9201T	Release 3, Version 1.20	DAS 9201T Application Software - 92DM911
X window on a workstation	Release 3, Version 1.20	DAS 92XTERM Application SW - 92DM911

*Version numbers shown are the lowest versions supported; higher version numbers within the same release are also supported.

If you have two types of DAS 9200 system software (9201T and 92XTerm), and you switch between the two, you must install compatible application software on each system.

If you try to install application software onto an incompatible system using DAS 9200 System Software Release 3, V1.1 or greater, an error message displays.

If you try to install application software onto an incompatible system using DAS 9200 System Software Release 3, V1.0 or lower, the system will install the software but it will not operate properly when you try to use it.

Install the disassembler software onto the DAS 9200 as follows:

1. Power up the DAS 9200 mainframe.
2. Insert the appropriate disk into the DAS 9200's floppy drive.
3. Press the Select Menu key and select the Disk Services menu.
4. Select Install Application in the Operation field of the menu.
5. Press F8: EXECUTE OPERATION and follow the on-screen prompts.

NOTE

After each install and load operation, a message appears on the screen informing you the operation succeeded or failed. If the message tells you the operation failed, you may need to remove applications or files from the hard disk and try installing or loading again. If the operation fails again, refer to Appendix A: Error Messages and Disassembly Problems.

CONNECTING TO THE SYSTEM UNDER TEST

Before you connect to the SUT, you must connect the standard probes to the 92A96 Module.

If your Futurebus+ system uses live-insertion filtering, refer to the description of *Jumpers* at the end of this section for information on live-insertion filtering and J4.

To connect the DAS 9200 to the SUT, do the following:

1. Turn off power to your SUT. It is not necessary to turn off power to the DAS 9200.

CAUTION

Static discharge can damage the probe adapter, the probes, or the 92A96 Module. To prevent static damage, handle the probe adapter, probes, and modules only in a static-free environment.

Always wear a grounding wrist strap or similar device while handling the probe adapter and Futurebus+ boards.

2. Attach a grounding strap between the ground jack on the back of the DAS 9200 and a ground point on the SUT.
3. To discharge your stored static electricity, touch the ground jack located on the back of the DAS 9200. Then, touch any of the ground pins of the probe adapter to discharge stored static electricity from the probe adapter.
4. Place the probe adapter onto a large piece of antistatic shipping foam to support the probe adapter as shown in Figure 2-3. This prevents the circuit board and its components from flexing.
5. To keep the probe adapter from teetering on the edge of the front panel as you connect the probes, place additional non-conductive material (such as foam) under the area to which the probes attach.
6. To connect the probes for each module, refer to Figure 2-3 and line up each probe with the corresponding section name printed on the probe adapter circuit board. The interface housing label indicates the group to which each clock and 8-channel probe connects. Ground pins are indicated on the board.

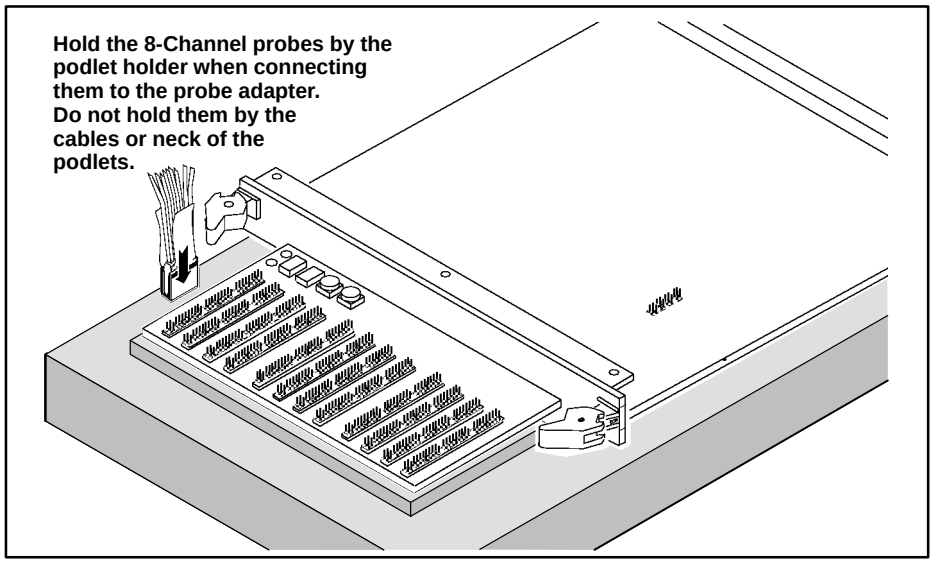


Figure 2-3. Connecting probes to the probe adapter.

CAUTION

*Live insertion of the probe adapter is **not** supported. To prevent damage to the probe adapter and Futurebus+ system, plug the probe adapter into the backplane when the Futurebus+ system is powered off.*

Failure to correctly place the probe adapter into the Futurebus+ backplane may damage the Futurebus+ system once power is applied.

After connecting the clock and 8-channel probes, you can install the probe adapter into your SUT as you would normally install any other Futurebus+ board. You can use the two yellow handles on the front panel of the probe adapter as needed when you install or remove the probe adapter.

To ensure that the probe adapter board is secure, tighten the screws under the yellow handles. Figure 2-4 shows the location of these screws.

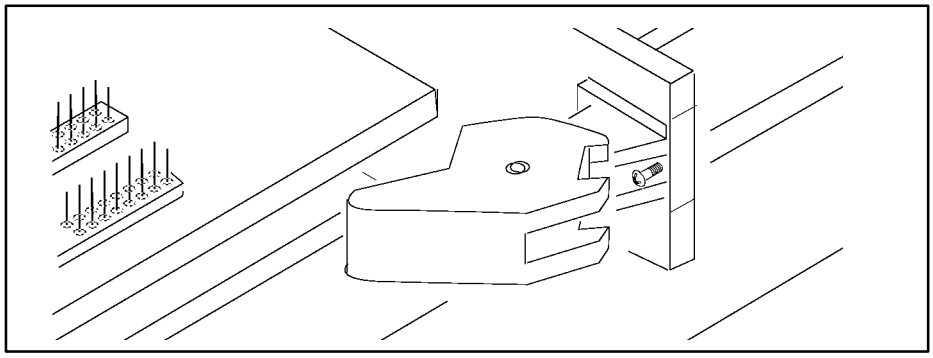


Figure 2-4. Location of screw under yellow handles.

CONFIGURING THE PROBE ADAPTER

There are two slide switches and two rotary switches on the probe adapter. The two slide switches are used to configure the probe adapter to acquire data from the Main or Arb buses for either synchronous (disassembly) or asynchronous (timing analysis) operation. One of the rotary switches is set to match the data path width of the Futurebus+ system backplane. The other rotary switch sets the glitch filter delay on the probe adapter.

Sync/Async Switches

The Sync/Async switches (S1 and S2) should be placed in the Sync position to acquire disassembly data, and in the Async position to acquire timing data. Use S1 to set probe adapter operation for the Main bus and S2 to set probe adapter operation for the Arb bus. Table 2-2 shows how to position these switches depending on the type of clocking you're using and the type of display you want to view.

Table 2-2
Sync/Async Switches Information

Switch Positions	Clocking	Display Menu
S1, Main bus		
Sync (Disassembly)	Custom	Disassembly, Timing, or State
	Internal*	Timing or State
Async (Timing)	Internal	Timing or State
S2, Arb bus		
Sync (Disassembly)†	External	Disassembly†, Timing or State
	Internal*	Timing or State
Async (Timing)	Internal	Timing or State

*Only useful for verifying probe adapter operation.
†Display of Arb bus data with Main bus disassembly requires clustering and correlating of the Arb bus module with the Main bus module.

Figure 2-5 shows the locations of S1 and S2 on the probe adapter.

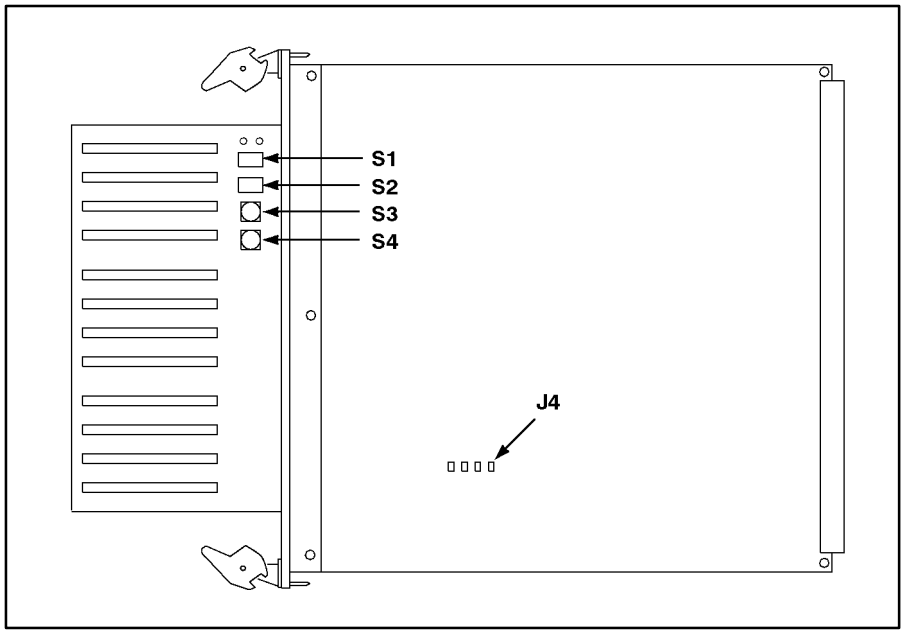


Figure 2-5. Switch locations on the probe adapter.

Glitch Filter Delay Switch

You can set the Glitch Filter Delay switch, S3, to an appropriate setting to match the characteristics of your Futurebus+ system backplane. Table 2-3 shows how to position this switch.

Table 2-3
Glitch Filter Delay Switch Positions

Switch Position	Nominal Delay*
0	13 ns
1	20 ns
2	27 ns
3	35 ns
*Twice the one-way backplane propagation delay.	

NOTE

*The operation of the Main and Arb bus logic on the probe adapter is **not** affected by this switch setting. Refer to Appendix C for more information about this switch.*

Figure 2-5 shows the location of S3 on the probe adapter.

Data Path Width Switch

You must set the Data Path Width switch, S4, to match the width of the data bus portion of the Futurebus+ system backplane to which the probe adapter connects. Switch positions are for 32-, 64-, and 128-bit wide data buses.

Figure 2-5 shows the location of S4 on the probe adapter.

Jumpers

Three jumpers, J1, J2, and J3, on the probe adapter should always be left open (no jumper). You cannot change the position of these jumpers and expect normal operation.

The last jumper, J4, controls whether live-insertion filtering is used in the acquisition of the AS* and DS* signals of the Main bus. These signals control the operation of the Main bus circuitry on the probe adapter. When J4 is not connected, filtering does not occur. When J4 is connected, filtering does occur.

Typically, J4 will not be connected unless you are using the probe adapter in a Futurebus+ system in which boards are installed and removed while the system is powered on. If you install or remove boards in your Futurebus+ system with power applied, then you should place a jumper on J4. Refer to Appendix C for more information on J4.

CAUTION

*Live insertion of the probe adapter is **not** supported. To prevent damage to the probe adapter and Futurebus+ system, plug the probe adapter into the backplane when the Futurebus+ system is powered off.*

NOTE

Do not install or remove J4 while the probe adapter is connected to a Futurebus+ system that is powered on; doing so may cause the Main bus circuitry on the probe adapter to enter an improper state.

If you change the jumper when the Futurebus+ system is powered on, you may have to reset the probe adapter circuitry.

The probe adapter can be reset in two ways. You can either power the Futurebus+ system off and then on, or you can momentarily short the POWERED signal of the probe adapter to ground. Table C-16 shows the channel assignment of the POWERED signal.

LED INDICATORS

There are two LEDs on the probe adapter. One lights when power is applied to the probe adapter, and the other lights when there is activity on the Futurebus+ bus.

The Power LED is red when the probe adapter is powered on. The Bus LED is yellow when either the AK* signal on the Main bus or the AP* signal on the Arb bus is asserted.

Figure 2-6 shows the location of these LEDs on the probe adapter.

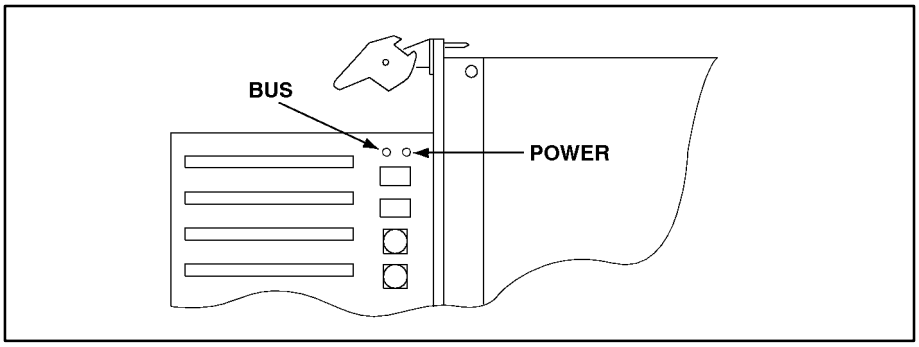


Figure 2-6. LED locations on the probe adapter.

Section 3: SETTING UP DISASSEMBLER SOFTWARE

This section tells how to prepare the disassembler software for acquiring data and discusses the following:

- supplied setups
- creating new setups
- channel groups and assignments
- changes that affect disassembly
- clocking
- symbols
- triggering

Before you acquire and disassemble data, you need to specify setups for clocking, triggering, and using symbols. The disassembly software provides default values for each of these setup controls, but you can change them as needed.

Table 3-1 shows the number of 92A96 Modules, the Futurebus+ buses they can support, and the name of the support or supplied setup you can use with each.

Table 3-1
Futurebus+ Supports and Supplied Setups

No. of Modules	Supported Futurebus+ Buses	Name of Support or Supplied Setup
1	Lower 64-bits* of the Main bus only†	FBus64 support
	Arb bus only	FB_1-A96 setup
2	128-bits* of the Main bus only	FBus+ support
	Lower 64-bits* of the Main bus† and Arb bus	FB_2-A96 setup
3	128-bits* of the Main bus and Arb bus	FB_3-A96 setup

*Or less
†Asynchronous control signals not available for timing analysis.

When you select a support type in the Software Support field of the 92A96 Configuration setup menu, the Channel, Clock, and Trigger menus are set up to support the probe adapter signals and switch settings. Acquired data is also disassembled when viewed in the Disassembly display.

A supplied setup allows you to restore previously saved setups for the Configuration, Channel, Clock, and Trigger menus. Clocking choices and disassembler support depend on the type of software support selected in the restored Configuration menu.

The two support types shown in Table 3-1 configure the DAS 9200 to acquire data from the Main bus only.

The three supplied setups shown in Table 3-1 configure the DAS 9200 to acquire data from the Arb bus only, or from both the Arb and Main buses. The Software Support field in the Configuration menu for the module acquiring Arb bus data is set to General Purpose. The Software Support field in the Configuration menu for the module acquiring Main bus data is set to either FBus+ or FBus64.

MODULE SUPPORT AND SUPPLIED SETUPS

The bus support product supplies the disassembler software and setup files for the module(s) to use to acquire and display Futurebus+ bus activity. Setup files are supplied for the Channel, Clock, and Trigger menus. Symbol files are supplied for displaying data and for use in the Trigger menu as word recognizer values. Timing format files are also provided for the Timing menu when performing timing analysis (described in Section 5).

You can select the disassembler (and its associated setup files) by selecting a type of Futurebus+ support, or by restoring a supplied setup file. Refer to the discussions on *Loading Support Software* and *Restoring Supplied Setups* later in this section for more information.

When there are two or three 92A96 Modules in adjacent slots, they are automatically formed into a variable-width module by the system software at power-on. You may have to reconfigure a variable-width module prior to selecting an appropriate software support in the 92A96 Configuration menu. If you restore a supplied cluster setup, the reconfiguration is done for you. Refer to the discussion of the System Configuration menu in the *DAS 9200 System User Manual* for details on how to reconfigure a variable-width module.

When you restore a supplied Futurebus+ multimodule setup, the DAS 9200 automatically does the following:

- reconfigures 92A96 Modules if the setup requires a variable-width module
- clusters and correlates 92A96 Modules if the setup requires a variable-width module clustered and correlated with another module
- selects the appropriate type of support for each of the modules

- defines two communication signals for use in the trigger programs of the modules called MainToArb and ArbToMain
- defines triggering for each module using the communication signals
- provides two predefined Timing Format Definition files, called FBus+_96, and FB+Arb_96

Full Main Bus and Arb Bus Supplied Setup

The FB_3-A96 setup requires three 92A96 Modules. When the setup is restored, a variable-width 92A96 Module is defined for the Main bus, which is clustered and correlated with a single 92A96 Module for the Arb bus. This setup configures the Channel, Clock, and Trigger menus of the DAS 9200 to acquire data from 128-bits (or less) of the Main bus and from the Arb bus.

Partial Main Bus and Arb Bus Supplied Setup

The FB_2-A96 setup requires two 92A96 Modules. When the setup is restored, the module for the Main bus is clustered and correlated with the module for the Arb bus. This setup also configures the Channel, Clock, and Trigger menus of the DAS 9200 to acquire data from 64-bits (or less) of the Main bus and from the Arb bus.

Full Main Bus Only Support

The FBus+ support software requires two 92A96 Modules formed into a variable-width module. When you access the Configuration menu and select Fbus+ in the Software Support field, the Channel, Clock, and Trigger menus for the variable-width module are set up to acquire data from 128-bits (or less) of the Main bus only.

Partial Main Bus Only Support

The FBus64 support software requires one 92A96 Module. When you access the Configuration menu and select Fbus64 in the Software Support field, the Channel, Clock, and Trigger menus for the module are set up to acquire data from the lower 64-bits (or less) of the Main bus only.

Arb Bus Only Supplied Setup

The FB_1-A96 setup requires one 92A96 Module. When the setup is restored, it configures the Channel, Clock, and Trigger menus to acquire data from the Arb bus only.

LOADING SUPPORT SOFTWARE

To load the FBus+ or FBus64 support, follow these steps:

1. Press the Menu Select key, select the Main bus module, select its Configuration menu, and press Return.
2. Select FBus+ or FBus64 support in the Software Support field.
3. Press F8: EXECUTE OPERATION.

When you load the support software, the Channel, Clock, and Trigger menus are automatically set up to acquire Main bus data from your Futurebus+ system. You can change the setups in the Clock and Trigger menus as needed. Refer to *Channel Groups and Assignments* in this section for information on what can be changed in the Channel menu.

RESTORING SUPPLIED SETUPS

To restore a supplied setup, refer to Figure 3-1 and follow these steps:

1. Press the Menu Select key, select the Save/Restore menu, and press Return.
2. Select Restore Setup (or Restore Partial Setup) in the Operation field.
3. Select the desired setup in the File field. The support software supplies three setup files: FB_1-A96, FB_2-A96, and FB_3-A96.
4. Press F8: EXECUTE OPERATION.

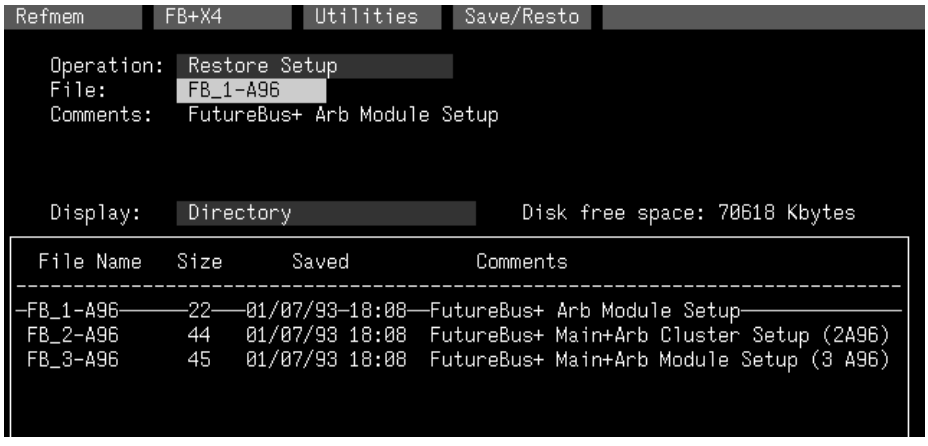


Figure 3-1. Save/Restore menu.

If you restored the FB_2-A96 or FB_3-A96 setup, the DAS 9200 automatically configures itself for multimodule operation. Refer to *Module Support and Supplied Setups* for a description of multimodule operation.

If the current placement of the data acquisition modules does not match that of the selected setup, the Restore Formation overlay appears. Press the F4: PLACE MODULES key or use the overlay to assign the module setups to the current placement of the modules.

If you are using 92A96D Modules when you restore a setup, the default acquisition memory depth is set to 8K. To use a greater memory depth, select a higher value in the Acquisition Memory Size field of the Configuration menu for each deep module.

CREATING MULTIMODULE SETUPS

You can create setups that meet the needs of your specific application. For example, you can create a setup that provides additional intermodule communication signals for use in complex trigger programs, or a setup to acquire data from multiple buses or other devices.

As you create a multimodule setup, keep in mind that Main and Arb bus modules must communicate with (signal to) each other, and that they must also start acquiring data at the same time. Therefore, you must set up the Main and Arb bus modules to be clustered and correlated, and you must also define signals for triggering purposes.

Before you can create a new setup using the Futurebus+ disassembler, you must first install the software and its associated files. Refer to the discussion on *Installing Software* in Section 2 for directions on how to do this.

The steps generally necessary to create your own setup are as follows:

- configure the DAS 9200 (if acquiring 128-bit wide Main bus data)
- restore an appropriate supplied setup or select a type of support
- name the modules
- cluster the modules
- correlate the modules
- define signals
- use signals in trigger programs (Trigger menu)
- set the start mode to ATE (Cluster menu)

Refer to your *DAS 9200 System User Manual* for information on how to perform these steps.

To restore a supplied setup, refer to the description of *Restoring Supplied Setups* earlier in this section.

CHANNEL GROUPS AND ASSIGNMENTS

The disassembler software automatically defines the channel groups for the Futurebus+ bus support. The channel groups for the Main bus are Ph, CM, AD63-32, AD31-0, BP7-0, CA, ST, D127-96, D95-64, BP15-8, TG, Async, and Filtered. The channel groups for the Arb bus are ArbAsync, ArbFiltered, AC, AB, and S1.

For the FBus+ disassembler to operate properly, the names and channel assignments of all Main groups above (except Async and Filtered) must not be changed. For the FBus64 disassembler, the name and channel assignments of the Ph, CM, AD63-32, AD31-0, BP7-0, CA, and ST channel groups must not be changed.

You can use channels from groups not used for disassembly to connect to other signals in your SUT. For example, you can use individual channels from the Async and Filtered groups to make other connections because these groups are not used for disassembly. You can also use channels from the AD63-32, BP7-4, D127-96, D95-64, BP15-8, and TG groups if you are not going to acquire bus data using these groups. If you want to know which signal is in which group, refer to the channel assignment tables in *Appendix C: Service Information*. Channel assignments are also shown in the Channel menu.

CHANGES THAT AFFECT DISASSEMBLY

You can change part of the default setups for the 92A96 Modules. However, keep in mind that if you change the threshold voltage (normally TTL, 1.5 V) or display polarity (normally +), the disassembled data will be affected.

CLOCKING

You can use the Clock menu to set clocking choices to control data sampling. The 92DM911 software offers a customized clocking selection for the Main bus of the Futurebus+ system. This clocking choice (Custom) is the default selection whenever you select the FBus64 or FBus+ Support in the Configuration menu.

Custom clocking is also the default selection for the Main bus when you restore any of the three supplied setup files. No Custom clocking selection is available for the Arb bus because there is no disassembler for the Arb bus. The Arb bus uses External clocking as the default selection when you restore any of the supplied setup files.

A description of how bus activity is sampled by the probe adapter is found in Appendix B.

Main Bus

The 92DM911 software provides two modes for acquiring Main bus data: Power-Up Cycles Acquired or Power-Up Cycles Not Acquired. The default is Power-Up Cycles Not Acquired. You can change the clocking mode by changing the Power-Up Cycles option field in the Clock menu. Figure 3-2 shows the default Clock menu setup for the Main bus module.

A power-up cycle is any cycle that occurs while the POWERED signal is false. This occurs when the Futurebus+ system is being powered-up or powered-down.

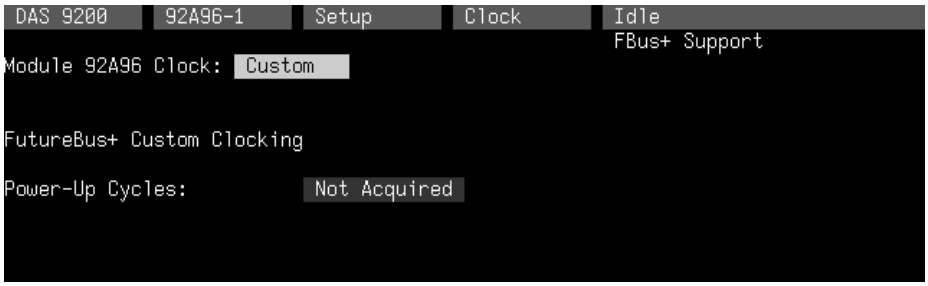


Figure 3-2. Default Clock menu for the Main bus module.

Disassembly will not be correct with the Internal or External clocking modes. Refer to *Section 4: General Purpose Analysis* for a description of using these other clock selections with this bus support package.

To select the clocking mode, do the following:

1. Press the Select Menu key.
2. Select the Clock menu for the Main bus module you want to use.
3. Select Custom clocking (the default with either support type selected in the Configuration menu).
4. Move the cursor to the Power-Up Cycles field and select one of the following types of clocking:
   - Acquired
   - Not Acquired

Arb Bus

No Custom clocking selection is available for the Arb bus because there is no disassembler for the Arb bus. The Arb bus uses External clocking as the default selection when you restore any of the supplied setup files. Figure 3-3 shows the default Clock menu for the Arb bus module.

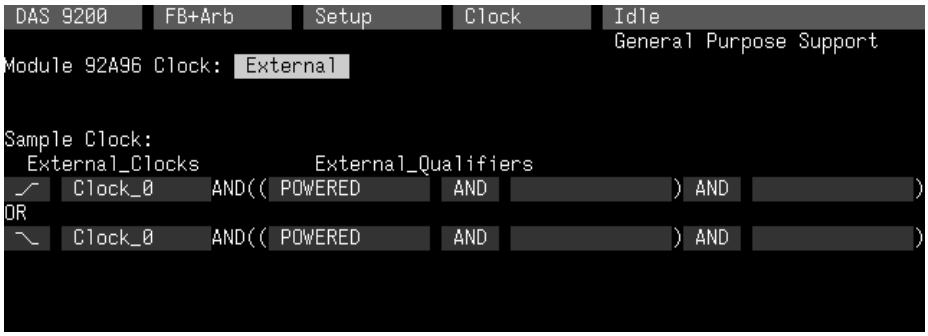


Figure 3-3. Default Clock menu for the Arb bus module.

SYMBOLS

Symbols can represent a set of specific channel group values or a range of channel group values (defined by upper and lower bounds).

You can use symbol tables to display channel group information symbolically in the State and Disassembly menus and to control triggering. There are three symbol table files supplied by the disassembler software to replace specific channel group values. Refer to *Triggering* in this section and *Displaying Channel Groups Symbolically* in Section 4 for more information on displaying symbolic values.

You can use the Symbol Editor to copy, rename, save, and modify any of the supplied symbol tables to suit your needs. Refer to *Copying and Editing Supplied Symbol Tables* later in this section for a description of how to do this.

When used in the State or Disassembly display, DAS 9200 system software searches for the first match value found in the symbol table and displays the corresponding symbol name.

Table 3-2 shows the name and bit pattern for the symbols in the file FB+_Ph, the Ph (phase) channel group symbol table.

Table 3-2
FB+_Ph Symbol Table

Symbol	Ph Group Value (POWERED L_CONN_1 L_CONN_0)	Symbol	Ph Group Value (POWERED L_CONN_1 L_CONN_0)
UnPd	0 X X	0X1	0 X 1
Lane	1 0 0	00X	0 0 X
Data	1 0 1	000	0 0 0
CONN	1 1 0	001	0 0 1
Disc	1 1 1	01X	0 1 X
XXX	X X X	010	0 1 0
XX0	X X 0	011	0 1 1
XX1	X X 1	1XX	1 X X
X0X	X 0 X	1X0	1 X 0
X00	X 0 0	1X1	1 X 1
X01	X 0 1	100	1 0 X
X1X	X 1 X	100	1 0 0
X10	X 1 0	101	1 0 1
X11	X 1 1	11X	1 1 X
0XX	0 X X	110	1 1 0
0X0	0 X 0	111	1 1 1

The UnPd symbol signifies a beat obtained during SUT power on or power off. The Lane symbol signifies the first data beat (lane deselection specification) of a partial transaction. The Data symbol signifies any other data beat. The CONN symbol signifies a connect beat. The Disc symbol signifies a disconnect beat.

Table 3-3 shows the signals that make up the CA group, and the meaning of each bit when it is asserted.

Table 3-3
CA Channel Group Bit Definitions

Signal Name	Abbreviation in Symbol and Meaning When Asserted
CA_2	Sr, a split response
CA_1	Co, a compelled transaction
CA_0	Ts, transmit speed low

Table 3-4 shows the name and bit pattern for the symbols in the file FB+_Cap, the CA channel group symbol table.

Table 3-4
FB+_Cap Symbol Table

Symbol	CA Group Value (CA_2 CA_1 CA_0)	Symbol	CA Group Value (CA_2 CA_1 CA_0)	Symbol	CA Group Value (CA_2 CA_1 CA_0)
	0 0 0	X00	X 0 0	010	0 1 0
Ts	0 0 1	X01	X 0 1	011	0 1 1
Co	0 1 0	X1X	X 1 X	1XX	1 X X
Co?Ts†	0 1 1	X10	X 1 0	1X0	1 X 0
Sr	1 0 0	X11	X 1 1	1X1	1 X 1
Sr, Ts	1 0 1	0XX	0 X X	10X	1 0 X
Sr, Co	1 1 0	0X0	0 X 0	100	1 0 0
?sct?†	1 1 1	0X1	0 X 1	101	1 0 1
XXX	X X X	00X	0 0 X	11X	1 1 X
XX0	X X 0	000	0 0 0	110	1 1 0
XX1	X X 1	001	0 0 1	111	1 1 1
X0X	X 0 X	01X	0 1 X		

†Not expected in normal Futurebus+ system operation.

Table 3-5 shows the signals that make up the ST group, the meaning of each bit when it is asserted, and the two- or one-letter abbreviation used in the symbol name.

Table 3-5
ST Channel Group Bit Definitions

Signal Name	Meaning When Asserted	2-Letter Abbreviation	1-Letter Abbreviation
ST_7	Wait	Wt	w
ST_6	Beat Error	Be	b
ST_5	Intervention	Iv	v
ST_4	Transaction Flag	Tf	f
ST_3	Broadcast/Broadcall	Bc	c
ST_2	Selected	Sl	s
ST_1	Busy or End of Data	Bs/Ed or Bd	y
ST_0	Transaction Error	Te	t

Table 3-6 shows the name and bit pattern for the symbols in the file FB+_Stat, the ST channel group symbol table.

As can be seen, the two-letter abbreviation will display for all asserted bits, separated by commas whenever there is enough space on the display to do so. As more bits are asserted, the commas will not display. And, as even more bits are asserted, only the one-letter abbreviation will display.

Although the meaning of ST_1 depends on when it was first asserted in the transaction (busy when asserted during a connect beat and end-of-data otherwise), the symbolic display of the ST channel group is only based on the value of the ST signals without consideration for the type of beat.

You may need to add additional symbols to a copy of the file to allow other ST values with several don’t care bits to be used for triggering. Refer to *Copying and Editing the Supplied Symbol Tables* in this section for information on how to do this.

Table 3-6
FB+_Stat Symbol Table Definitions

Symbol	ST Group Value (ST_7 ST_6 ST_5 ST_4 ST_3 ST_2 ST_1 ST_0)	Symbol	ST Group Value (ST_7 ST_6 ST_5 ST_4 ST_3 ST_2 ST_1 ST_0)	Symbol	ST Group Value (ST_7 ST_6 ST_5 ST_4 ST_3 ST_2 ST_1 ST_0)
	0 0 0 0 0 0 0 0	Iv	0 0 1 0 0 0 0 0	Be	0 1 0 0 0 0 0 0
Te	0 0 0 0 0 0 0 1	Iv,Te	0 0 1 0 0 0 0 1	Be,Te	0 1 0 0 0 0 0 1
Bs/Ed	0 0 0 0 0 0 1 0	Iv,Bs/Ed	0 0 1 0 0 0 1 0	Be,Bs/Ed	0 1 0 0 0 0 1 0
Bs/Ed,Te	0 0 0 0 0 0 1 1	Iv,Bd,Te	0 0 1 0 0 0 1 1	Be,Bd,Te	0 1 0 0 0 0 1 1
Sl	0 0 0 0 0 1 0 0	Iv,Sl	0 0 1 0 0 1 0 0	Be,Sl	0 1 0 0 0 1 0 0
Sl,Te	0 0 0 0 0 1 0 1	Iv,Sl,Te	0 0 1 0 0 1 0 1	Be,Sl,Te	0 1 0 0 0 1 0 1
Sl,Bs/Ed	0 0 0 0 0 1 1 0	Iv,Sl.Bd	0 0 1 0 0 1 1 0	Be,Sl,Bd	0 1 0 0 0 1 1 0
Sl,Bd,Te	0 0 0 0 0 1 1 1	IvSlBdTe	0 0 1 0 0 1 1 1	BeSlBdTe	0 1 0 0 0 1 1 1
Bc	0 0 0 0 1 0 0 0	Iv,Bc	0 0 1 0 1 0 0 0	Be,Bc	0 1 0 0 1 0 0 0
Bc,Te	0 0 0 0 1 0 0 1	Iv,Bc,Te	0 0 1 0 1 0 0 1	Be,Bc,Te	0 1 0 0 1 0 0 1
Bc,Bs/Ed	0 0 0 0 1 0 1 0	Iv,Bc,Bd	0 0 1 0 1 0 1 0	Be,Bc,Bd	0 1 0 0 1 0 1 0
Bc,Bd,Te	0 0 0 0 1 0 1 1	IvBcBdTe	0 0 1 0 1 0 1 1	BeBcBdTe	0 1 0 0 1 0 1 1
Bc,Sl	0 0 0 0 1 1 0 0	Iv,Bc,Sl	0 0 1 0 1 1 0 0	Be,Bc,Sl	0 1 0 0 1 1 0 0
Bc,Sl,Te	0 0 0 0 1 1 0 1	IvBcSlTe	0 0 1 0 1 1 0 1	BeBcSlTe	0 1 0 0 1 1 0 1
Bc,Sl,Bd	0 0 0 0 1 1 1 0	IvBcSlBd	0 0 1 0 1 1 1 0	BeBcSlBd	0 1 0 0 1 1 1 0
BcSlBdTe	0 0 0 0 1 1 1 1	--v-csyt	0 0 1 0 1 1 1 1	-b--csyt	0 1 0 0 1 1 1 1
Tf	0 0 0 1 0 0 0 0	Iv,Tf	0 0 1 1 0 0 0 0	Be,Tf	0 1 0 1 0 0 0 0
Tf,Te	0 0 0 1 0 0 0 1	Iv,Tf,Te	0 0 1 1 0 0 0 1	Be,Tf,Te	0 1 0 1 0 0 0 1
Tf,Bs/Ed	0 0 0 1 0 0 1 0	Iv,Tf,Bd	0 0 1 1 0 0 1 0	Be,Tf,Bd	0 1 0 1 0 0 1 0
Tf,Bd,Te	0 0 0 1 0 0 1 1	IvTfBdTe	0 0 1 1 0 0 1 1	BeTfBdTe	0 1 0 1 0 0 1 1
Tf,Sl	0 0 0 1 0 1 0 0	Iv,Tf,Sl	0 0 1 1 0 1 0 0	Be,Tf,Sl	0 1 0 1 0 1 0 0
Tf,Sl,Te	0 0 0 1 0 1 0 1	IvTfSlTe	0 0 1 1 0 1 0 1	BeTfSlTe	0 1 0 1 0 1 0 1
Tf,Sl,Bd	0 0 0 1 0 1 1 0	IvTfSlBd	0 0 1 1 0 1 1 0	BeTfSlBd	0 1 0 1 0 1 1 0
TfSlBdTe	0 0 0 1 0 1 1 1	--vf-syt	0 0 1 1 0 1 1 1	-b-f-syt	0 1 0 1 0 1 1 1
Tf,Bc	0 0 0 1 1 0 0 0	Iv,Tf,Bc	0 0 1 1 1 0 0 0	Be,Tf,Bc	0 1 0 1 1 0 0 0
Tf,Bc,Te	0 0 0 1 1 0 0 1	IvTfBcTe	0 0 1 1 1 0 0 1	BeTfBcTe	0 1 0 1 1 0 0 1
Tf,Bc,Bd	0 0 0 1 1 0 1 0	IvTfBcBd	0 0 1 1 1 0 1 0	BeTfBcBd	0 1 0 1 1 0 1 0
TfBcBdTe	0 0 0 1 1 0 1 1	--vfc-yt	0 0 1 1 1 0 1 1	-b-fc-yt	0 1 0 1 1 0 1 1
Tf,Bc,Sl	0 0 0 1 1 1 0 0	IvTfBcSl	0 0 1 1 1 1 0 0	BeTfBcSl	0 1 0 1 1 1 0 0
TfBcSlTe	0 0 0 1 1 1 0 1	--vfcs-t	0 0 1 1 1 1 0 1	-b-fcs-t	0 1 0 1 1 1 0 1
TfBcSlBd	0 0 0 1 1 1 1 0	--vfcsy-	0 0 1 1 1 1 1 0	-b-fcsy-	0 1 0 1 1 1 1 0
---fcsyt	0 0 0 1 1 1 1 1	--vfcsyt	0 0 1 1 1 1 1 1	-b-fcsyt	0 1 0 1 1 1 1 1

(Cont.)

Table 3-6 (Cont.)
FB+_Stat Symbol Table Definitions

Symbol	ST Group Value (ST_7 ST_6 ST_5 ST_4 ST_3 ST_2 ST_1 ST_0)	Symbol	ST Group Value (ST_7 ST_6 ST_5 ST_4 ST_3 ST_2 ST_1 ST_0)	Symbol	ST Group Value (ST_7 ST_6 ST_5 ST_4 ST_3 ST_2 ST_1 ST_0)
Be,Iv	0 1 1 0 0 0 0 0	Wt	1 0 0 0 0 0 0 0	Wt,Iv	1 0 1 0 0 0 0 0
Be,Iv,Te	0 1 1 0 0 0 0 1	Wt,Te	1 0 0 0 0 0 0 1	Wt,Iv,Te	1 0 1 0 0 0 0 1
Be,Iv,Bd	0 1 1 0 0 0 1 0	Wt,Bs/Ed	1 0 0 0 0 0 1 0	Wt,Iv,Bd	1 0 1 0 0 0 1 0
BeIvBdTe	0 1 1 0 0 0 1 1	Wt,Bd,Te	1 0 0 0 0 0 1 1	WtIvBdTe	1 0 1 0 0 0 1 1
Be,Iv,Sl	0 1 1 0 0 1 0 0	Wt,Sl	1 0 0 0 0 1 0 0	Wt,Iv,Sl	1 0 1 0 0 1 0 0
BeIvSlTe	0 1 1 0 0 1 0 1	Wt,Sl,Te	1 0 0 0 0 1 0 1	WtIvSlTe	1 0 1 0 0 1 0 1
BeIvSlBd	0 1 1 0 0 1 1 0	Wt,Sl,Bd	1 0 0 0 0 1 1 0	WtIvSlBd	1 0 1 0 0 1 1 0
-bv--syt	0 1 1 0 0 1 1 1	WtSlBdTe	1 0 0 0 0 1 1 1	w-v--syt	1 0 1 0 0 1 1 1
Be,Iv,Bc	0 1 1 0 1 0 0 0	Wt,Bc	1 0 0 0 1 0 0 0	Wt,Iv,Bc	1 0 1 0 1 0 0 0
BeIvBcTe	0 1 1 0 1 0 0 1	Wt,Bc,Te	1 0 0 0 1 0 0 1	WtIvBcTe	1 0 1 0 1 0 0 1
BeIvBcBd	0 1 1 0 1 0 1 0	Wt,Bc,Bd	1 0 0 0 1 0 1 0	WtIvBcBd	1 0 1 0 1 0 1 0
-bv-c-yt	0 1 1 0 1 0 1 1	WtBcBdTe	1 0 0 0 1 0 1 1	w-v-c-yt	1 0 1 0 1 0 1 1
BeIvBcSl	0 1 1 0 1 1 0 0	Wt,Bc,Sl	1 0 0 0 1 1 0 0	WtIvBcSl	1 0 1 0 1 1 0 0
-bv-cs-t	0 1 1 0 1 1 0 1	WtBcSlTe	1 0 0 0 1 1 0 1	w-v-cs-t	1 0 1 0 1 1 0 1
-bv-csy-	0 1 1 0 1 1 1 0	WtBcSlBd	1 0 0 0 1 1 1 0	w-v-csy-	1 0 1 0 1 1 1 0
-bv-csyt	0 1 1 0 1 1 1 1	w---csyt	1 0 0 0 1 1 1 1	w-v-csyt	1 0 1 0 1 1 1 1
Be,Iv,Tf	0 1 1 1 0 0 0 0	Wt,Tf	1 0 0 1 0 0 0 0	Wt,Iv,Tf	1 0 1 1 0 0 0 0
BeIvTfTe	0 1 1 1 0 0 0 1	Wt,Tf,Te	1 0 0 1 0 0 0 1	WtIvTfTe	1 0 1 1 0 0 0 1
BeIvTfBd	0 1 1 1 0 0 1 0	Wt,Tf,Bd	1 0 0 1 0 0 1 0	WtIvTfBd	1 0 1 1 0 0 1 0
-bvf--yt	0 1 1 1 0 0 1 1	WtTfBdTe	1 0 0 1 0 0 1 1	w-vf--yt	1 0 1 1 0 0 1 1
BeIvTfSl	0 1 1 1 0 1 0 0	Wt,Tf,sl	1 0 0 1 0 1 0 0	WtIvTfSl	1 0 1 1 0 1 0 0
-bvf-s-t	0 1 1 1 0 1 0 1	WtTfSlTe	1 0 0 1 0 1 0 1	w-vf-s-t	1 0 1 1 0 1 0 1
-bvf-sy-	0 1 1 1 0 1 1 0	WtTfSlBd	1 0 0 1 0 1 1 0	w-vf-sy-	1 0 1 1 0 1 1 0
-bvf-syt	0 1 1 1 0 1 1 1	w--f-syt	1 0 0 1 0 1 1 1	w-vf-syt	1 0 1 1 0 1 1 1
BeIvTfBc	0 1 1 1 1 0 0 0	Wt,Tf,Bc	1 0 0 1 1 0 0 0	WtIvTfBc	1 0 1 1 1 0 0 0
-bvfc--t	0 1 1 1 1 0 0 1	WtTfBcTe	1 0 0 1 1 0 0 1	w-vfc--t	1 0 1 1 1 0 0 1
-bvfc-y-	0 1 1 1 1 0 1 0	WtTfBcBd	1 0 0 1 1 0 1 0	w-vfc-y-	1 0 1 1 1 0 1 0
-bvfc-yt	0 1 1 1 1 0 1 1	w--fc-yt	1 0 0 1 1 0 1 1	w-vfc-yt	1 0 1 1 1 0 1 1
-bvfcs--	0 1 1 1 1 1 0 0	WtTfBcSl	1 0 0 1 1 1 0 0	w-vfcs--	1 0 1 1 1 1 0 0
-bvfcs-t	0 1 1 1 1 1 0 1	w--fcs-t	1 0 0 1 1 1 0 1	w-vfcs-t	1 0 1 1 1 1 0 1
-bvfcsy-	0 1 1 1 1 1 1 0	w--fcsy-	1 0 0 1 1 1 1 0	w-vfcsy-	1 0 1 1 1 1 1 0
-bvfcsyt	0 1 1 1 1 1 1 1	w--fcsyt	1 0 0 1 1 1 1 1	w-vfcsyt	1 0 1 1 1 1 1 1

(Cont.)

Table 3-6 (Cont.)
FB+_Stat Symbol Table Definitions

Symbol	ST Group Value (ST_7 ST_6 ST_5 ST_4 ST_3 ST_2 ST_1 ST_0)	Symbol	ST Group Value (ST_7 ST_6 ST_5 ST_4 ST_3 ST_2 ST_1 ST_0)	Symbol	ST Group Value (ST_7 ST_6 ST_5 ST_4 ST_3 ST_2 ST_1 ST_0)
Wt,Be	1 1 0 0 0 0 0 0	Wt,BeIv	1 1 1 0 0 0 0 0	--------	0 0 0 0 0 0 0 0
Wt,Be,Te	1 1 0 0 0 0 0 1	WtBeIvTe	1 1 1 0 0 0 0 1	-------t	0 0 0 0 0 0 0 1
Wt,Be,Bd	1 1 0 0 0 0 1 0	WtBeIvBd	1 1 1 0 0 0 1 0	------y-	0 0 0 0 0 0 1 0
WtBeBdTe	1 1 0 0 0 0 1 1	wbv---yt	1 1 1 0 0 0 1 1	------yt	0 0 0 0 0 0 1 1
Wt,Be,Sl	1 1 0 0 0 1 0 0	WtBeIvSl	1 1 1 0 0 1 0 0	-----s--	0 0 0 0 0 1 0 0
WtBeSlTe	1 1 0 0 0 1 0 1	wbv--s-t	1 1 1 0 0 1 0 1	-----s-t	0 0 0 0 0 1 0 1
WtBeSlBd	1 1 0 0 0 1 1 0	wbv--sy-	1 1 1 0 0 1 1 0	-----sy-	0 0 0 0 0 1 1 0
wb---syt	1 1 0 0 0 1 1 1	wbv--syt	1 1 1 0 0 1 1 1	-----syt	0 0 0 0 0 1 1 1
Wt,Be,Bc	1 1 0 0 1 0 0 0	WtBeIvBc	1 1 1 0 1 0 0 0	----c---	0 0 0 0 1 0 0 0
WtBeBcTe	1 1 0 0 1 0 0 1	wbv-c--t	1 1 1 0 1 0 0 1	----c--t	0 0 0 0 1 0 0 1
WtBeBcBd	1 1 0 0 1 0 1 0	wbv-c-y-	1 1 1 0 1 0 1 0	----c-y-	0 0 0 0 1 0 1 0
wb--c-yt	1 1 0 0 1 0 1 1	wbv-c-yt	1 1 1 0 1 0 1 1	----c-yt	0 0 0 0 1 0 1 1
WtBeBcSl	1 1 0 0 1 1 0 0	wbv-cs--	1 1 1 0 1 1 0 0	----cs--	0 0 0 0 1 1 0 0
wb--cs-t	1 1 0 0 1 1 0 1	wbv-cs-t	1 1 1 0 1 1 0 1	----cs-t	0 0 0 0 1 1 0 1
wb--csy-	1 1 0 0 1 1 1 0	wbv-csy-	1 1 1 0 1 1 1 0	----csy-	0 0 0 0 1 1 1 0
wb--csyt	1 1 0 0 1 1 1 1	wbv-csyt	1 1 1 0 1 1 1 1	----csyt	0 0 0 0 1 1 1 1
Wt,Be,Tf	1 1 0 1 0 0 0 0	WtBeIvTf	1 1 1 1 0 0 0 0	---f----	0 0 0 1 0 0 0 0
WtBeTfTe	1 1 0 1 0 0 0 1	wbvf---t	1 1 1 1 0 0 0 1	---f---t	0 0 0 1 0 0 0 1
WtBeTfBd	1 1 0 1 0 0 1 0	wbvf--y-	1 1 1 1 0 0 1 0	---f--y-	0 0 0 1 0 0 1 0
wb-f--yt	1 1 0 1 0 0 1 1	wbvf--yt	1 1 1 1 0 0 1 1	---f--yt	0 0 0 1 0 0 1 1
wb-f-s--	1 1 0 1 0 1 0 0	wbvf-s--	1 1 1 1 0 1 0 0	---f-s--	0 0 0 1 0 1 0 0
wb-f-s-t	1 1 0 1 0 1 0 1	wbvf-s-t	1 1 1 1 0 1 0 1	---f-s-t	0 0 0 1 0 1 0 1
wb-f-sy-	1 1 0 1 0 1 1 0	wbvf-sy-	1 1 1 1 0 1 1 0	---f-sy-	0 0 0 1 0 1 1 0
wb-f-syt	1 1 0 1 0 1 1 1	wbvf-syt	1 1 1 1 0 1 1 1	---f-syt	0 0 0 1 0 1 1 1
WtBeTfBc	1 1 0 1 1 0 0 0	wbvfc---	1 1 1 1 1 0 0 0	---fc---	0 0 0 1 1 0 0 0
wb-fc--t	1 1 0 1 1 0 0 1	wbvfc--t	1 1 1 1 1 0 0 1	---fc--t	0 0 0 1 1 0 0 1
wb-fc-y-	1 1 0 1 1 0 1 0	wbvfc-y-	1 1 1 1 1 0 1 0	---fc-y-	0 0 0 1 1 0 1 0
wb-fc-yt	1 1 0 1 1 0 1 1	wbvfc-yt	1 1 1 1 1 0 1 1	---fc-yt	0 0 0 1 1 0 1 1
wb-fcs--	1 1 0 1 1 1 0 0	wbvfcs--	1 1 1 1 1 1 0 0	---fcs--	0 0 0 1 1 1 0 0
wb-fcs-t	1 1 0 1 1 1 0 1	wbvfcs-t	1 1 1 1 1 1 0 1	---fcs-t	0 0 0 1 1 1 0 1
wb-fcsy-	1 1 0 1 1 1 1 0	wbvfcsy-	1 1 1 1 1 1 1 0	---fcsy-	0 0 0 1 1 1 1 0
wb-fcsyt	1 1 0 1 1 1 1 1	wbvfcsyt	1 1 1 1 1 1 1 1	---fcsyt	0 0 0 1 1 1 1 1

(Cont.)

Table 3-6 (Cont.)
FB+_Stat Symbol Table Definitions

Symbol	ST Group Value (ST_7 ST_6 ST_5 ST_4 ST_3 ST_2 ST_1 ST_0)	Symbol	ST Group Value (ST_7 ST_6 ST_5 ST_4 ST_3 ST_2 ST_1 ST_0)	Symbol	ST Group Value (ST_7 ST_6 ST_5 ST_4 ST_3 ST_2 ST_1 ST_0)
--v-----	0 0 1 0 0 0 0 0	-b------	0 1 0 0 0 0 0 0	-bv-----	0 1 1 0 0 0 0 0
--v----t	0 0 1 0 0 0 0 1	-b-----t	0 1 0 0 0 0 0 1	-bv----t	0 1 1 0 0 0 0 1
--v---y-	0 0 1 0 0 0 1 0	-b----y-	0 1 0 0 0 0 1 0	-bv---y-	0 1 1 0 0 0 1 0
--v---yt	0 0 1 0 0 0 1 1	-b----yt	0 1 0 0 0 0 1 1	-bv---yt	0 1 1 0 0 0 1 1
--v--s--	0 0 1 0 0 1 0 0	-b---s--	0 1 0 0 0 1 0 0	-bv--s--	0 1 1 0 0 1 0 0
--v--s-t	0 0 1 0 0 1 0 1	-b---s-t	0 1 0 0 0 1 0 1	-bv--s-t	0 1 1 0 0 1 0 1
--v--sy-	0 0 1 0 0 1 1 0	-b---sy-	0 1 0 0 0 1 1 0	-bv--sy-	0 1 1 0 0 1 1 0
--v--syt	0 0 1 0 0 1 1 1	-b---syt	0 1 0 0 0 1 1 1	-bv--syt	0 1 1 0 0 1 1 1
--v-c---	0 0 1 0 1 0 0 0	-b--c---	0 1 0 0 1 0 0 0	-bv-c---	0 1 1 0 1 0 0 0
--v-c--t	0 0 1 0 1 0 0 1	-b--c--t	0 1 0 0 1 0 0 1	-bv-c--t	0 1 1 0 1 0 0 1
--v-c-y-	0 0 1 0 1 0 1 0	-b--c-y-	0 1 0 0 1 0 1 0	-bv-c-y-	0 1 1 0 1 0 1 0
--v-c-yt	0 0 1 0 1 0 1 1	-b--c-yt	0 1 0 0 1 0 1 1	-bv-c-yt	0 1 1 0 1 0 1 1
--v-cs--	0 0 1 0 1 1 0 0	-b--cs--	0 1 0 0 1 1 0 0	-bv-cs--	0 1 1 0 1 1 0 0
--v-cs-t	0 0 1 0 1 1 0 1	-b--cs-t	0 1 0 0 1 1 0 1	-bv-cs-t	0 1 1 0 1 1 0 1
--v-csy-	0 0 1 0 1 1 1 0	-b--csy-	0 1 0 0 1 1 1 0	-bv-csy-	0 1 1 0 1 1 1 0
--v-csyt	0 0 1 0 1 1 1 1	-b--csyt	0 1 0 0 1 1 1 1	-bv-csyt	0 1 1 0 1 1 1 1
--vf----	0 0 1 1 0 0 0 0	-b-f----	0 1 0 1 0 0 0 0	-bvf----	0 1 1 1 0 0 0 0
--vf---t	0 0 1 1 0 0 0 1	-b-f---t	0 1 0 1 0 0 0 1	-bvf---t	0 1 1 1 0 0 0 1
--vf--y-	0 0 1 1 0 0 1 0	-b-f--y-	0 1 0 1 0 0 1 0	-bvf--y-	0 1 1 1 0 0 1 0
--vf--yt	0 0 1 1 0 0 1 1	-b-f--yt	0 1 0 1 0 0 1 1	-bvf--yt	0 1 1 1 0 0 1 1
--vf-s--	0 0 1 1 0 1 0 0	-b-f-s--	0 1 0 1 0 1 0 0	-bvf-s--	0 1 1 1 0 1 0 0
--vf-s-t	0 0 1 1 0 1 0 1	-b-f-s-t	0 1 0 1 0 1 0 1	-bvf-s-t	0 1 1 1 0 1 0 1
--vf-sy-	0 0 1 1 0 1 1 0	-b-f-sy-	0 1 0 1 0 1 1 0	-bvf-sy-	0 1 1 1 0 1 1 0
--vf-syt	0 0 1 1 0 1 1 1	-b-f-syt	0 1 0 1 0 1 1 1	-bvf-syt	0 1 1 1 0 1 1 1
--vfc---	0 0 1 1 1 0 0 0	-b-fc---	0 1 0 1 1 0 0 0	-bvfc---	0 1 1 1 1 0 0 0
--vfc--t	0 0 1 1 1 0 0 1	-b-fc--t	0 1 0 1 1 0 0 1	-bvfc--t	0 1 1 1 1 0 0 1
--vfc-y-	0 0 1 1 1 0 1 0	-b-fc-y-	0 1 0 1 1 0 1 0	-bvfc-y-	0 1 1 1 1 0 1 0
--vfc-yt	0 0 1 1 1 0 1 1	-b-fc-yt	0 1 0 1 1 0 1 1	-bvfc-yt	0 1 1 1 1 0 1 1
--vfcs--	0 0 1 1 1 1 0 0	-b-fcs--	0 1 0 1 1 1 0 0	-bvfcs--	0 1 1 1 1 1 0 0
--vfcs-t	0 0 1 1 1 1 0 1	-b-fcs-t	0 1 0 1 1 1 0 1	-bvfcs-t	0 1 1 1 1 1 0 1
--vfcsy-	0 0 1 1 1 1 1 0	-b-fcsy-	0 1 0 1 1 1 1 0	-bvfcsy-	0 1 1 1 1 1 1 0
--vfcsyt	0 0 1 1 1 1 1 1	-b-fcsyt	0 1 0 1 1 1 1 1	-bvfcsyt	0 1 1 1 1 1 1 1

(Cont.)

Table 3-6 (Cont.)
FB+_Stat Symbol Table Definitions

Symbol	ST Group Value (ST_7 ST_6 ST_5 ST_4 ST_3 ST_2 ST_1 ST_0)	Symbol	ST Group Value (ST_7 ST_6 ST_5 ST_4 ST_3 ST_2 ST_1 ST_0)	Symbol	ST Group Value (ST_7 ST_6 ST_5 ST_4 ST_3 ST_2 ST_1 ST_0)
w-------	1 0 0 0 0 0 0 0	w-v-----	1 0 1 0 0 0 0 0	wb------	1 1 0 0 0 0 0 0
w------t	1 0 0 0 0 0 0 1	w-v----t	1 0 1 0 0 0 0 1	wb-----t	1 1 0 0 0 0 0 1
w-----y-	1 0 0 0 0 0 1 0	w-v---y-	1 0 1 0 0 0 1 0	wb----y-	1 1 0 0 0 0 1 0
w-----yt	1 0 0 0 0 0 1 1	w-v---yt	1 0 1 0 0 0 1 1	wb----yt	1 1 0 0 0 0 1 1
w----s--	1 0 0 0 0 1 0 0	w-v--s--	1 0 1 0 0 1 0 0	wb---s--	1 1 0 0 0 1 0 0
w----s-t	1 0 0 0 0 1 0 1	w-v--s-t	1 0 1 0 0 1 0 1	wb---s-t	1 1 0 0 0 1 0 1
w----sy-	1 0 0 0 0 1 1 0	w-v--sy-	1 0 1 0 0 1 1 0	wb---sy-	1 1 0 0 0 1 1 0
w----syt	1 0 0 0 0 1 1 1	w-v--syt	1 0 1 0 0 1 1 1	wb---syt	1 1 0 0 0 1 1 1
w---c---	1 0 0 0 1 0 0 0	w-v-c---	1 0 1 0 1 0 0 0	wb--c---	1 1 0 0 1 0 0 0
w---c--t	1 0 0 0 1 0 0 1	w-v-c--t	1 0 1 0 1 0 0 1	wb--c--t	1 1 0 0 1 0 0 1
w---c-y-	1 0 0 0 1 0 1 0	w-v-c-y-	1 0 1 0 1 0 1 0	wb--c-y-	1 1 0 0 1 0 1 0
w---c-yt	1 0 0 0 1 0 1 1	w-v-c-yt	1 0 1 0 1 0 1 1	wb--c-yt	1 1 0 0 1 0 1 1
w---cs--	1 0 0 0 1 1 0 0	w-v-cs--	1 0 1 0 1 1 0 0	wb--cs--	1 1 0 0 1 1 0 0
w---cs-t	1 0 0 0 1 1 0 1	w-v-cs-t	1 0 1 0 1 1 0 1	wb--cs-t	1 1 0 0 1 1 0 1
w---csy-	1 0 0 0 1 1 1 0	w-v-csy-	1 0 1 0 1 1 1 0	wb--csy-	1 1 0 0 1 1 1 0
w---csyt	1 0 0 0 1 1 1 1	w-v-csyt	1 0 1 0 1 1 1 1	wb--csyt	1 1 0 0 1 1 1 1
w--f----	1 0 0 1 0 0 0 0	w-vf----	1 0 1 1 0 0 0 0	wb-f----	1 1 0 1 0 0 0 0
w--f---t	1 0 0 1 0 0 0 1	w-vf---t	1 0 1 1 0 0 0 1	wb-f---t	1 1 0 1 0 0 0 1
w--f--y-	1 0 0 1 0 0 1 0	w-vf--y-	1 0 1 1 0 0 1 0	wb-f--y-	1 1 0 1 0 0 1 0
w--f--yt	1 0 0 1 0 0 1 1	w-vf--yt	1 0 1 1 0 0 1 1	wb-f--yt	1 1 0 1 0 0 1 1
w--f-s--	1 0 0 1 0 1 0 0	w-vf-s--	1 0 1 1 0 1 0 0	wb-f-s--	1 1 0 1 0 1 0 0
w--f-s-t	1 0 0 1 0 1 0 1	w-vf-s-t	1 0 1 1 0 1 0 1	wb-f-s-t	1 1 0 1 0 1 0 1
w--f-sy-	1 0 0 1 0 1 1 0	w-vf-sy-	1 0 1 1 0 1 1 0	wb-f-sy-	1 1 0 1 0 1 1 0
w--f-syt	1 0 0 1 0 1 1 1	w-vf-syt	1 0 1 1 0 1 1 1	wb-f-syt	1 1 0 1 0 1 1 1
w--fc---	1 0 0 1 1 0 0 0	w-vfc---	1 0 1 1 1 0 0 0	wb-fc---	1 1 0 1 1 0 0 0
w--fc--t	1 0 0 1 1 0 0 1	w-vfc--t	1 0 1 1 1 0 0 1	wb-fc--t	1 1 0 1 1 0 0 1
w--fc-y-	1 0 0 1 1 0 1 0	w-vfc-y-	1 0 1 1 1 0 1 0	wb-fc-y-	1 1 0 1 1 0 1 0
w--fc-yt	1 0 0 1 1 0 1 1	w-vfc-yt	1 0 1 1 1 0 1 1	wb-fc-yt	1 1 0 1 1 0 1 1
w--fcs--	1 0 0 1 1 1 0 0	w-vfcs--	1 0 1 1 1 1 0 0	wb-fcs--	1 1 0 1 1 1 0 0
w--fcs-t	1 0 0 1 1 1 0 1	w-vfcs-t	1 0 1 1 1 1 0 1	wb-fcs-t	1 1 0 1 1 1 0 1
w--fcsy-	1 0 0 1 1 1 1 0	w-vfcsy-	1 0 1 1 1 1 1 0	wb-fcsy-	1 1 0 1 1 1 1 0
w--fcsyt	1 0 0 1 1 1 1 1	w-vfcsyt	1 0 1 1 1 1 1 1	wb-fcsyt	1 1 0 1 1 1 1 1

(Cont.)

Table 3-6 (Cont.)
FB+_Stat Symbol Table Definitions

Symbol	ST Group Value (ST_7 ST_6 ST_5 ST_4 ST_3 ST_2 ST_1 ST_0)	Symbol	ST Group Value (ST_7 ST_6 ST_5 ST_4 ST_3 ST_2 ST_1 ST_0)
wbv-----	1 1 1 0 0 0 0 0	00000000	0 0 0 0 0 0 0 0
wbv----t	1 1 1 0 0 0 0 1	00000001	0 0 0 0 0 0 0 1
wbv---y-	1 1 1 0 0 0 1 0	0000000X	0 0 0 0 0 0 0 X
wbv---yt	1 1 1 0 0 0 1 1	00000010	0 0 0 0 0 0 1 0
wbv--s--	1 1 1 0 0 1 0 0	000000X0	0 0 0 0 0 0 X 0
wbv--s-t	1 1 1 0 0 1 0 1	00000100	0 0 0 0 0 1 0 0
wbv--sy-	1 1 1 0 0 1 1 0	00000X00	0 0 0 0 0 X 0 0
wbv--syt	1 1 1 0 0 1 1 1	00001000	0 0 0 0 1 0 0 0
wbv-c---	1 1 1 0 1 0 0 0	0000X000	0 0 0 0 X 0 0 0
wbv-c--t	1 1 1 0 1 0 0 1	00010000	0 0 0 1 0 0 0 0
wbv-c-y-	1 1 1 0 1 0 1 0	000X0000	0 0 0 X 0 0 0 0
wbv-c-yt	1 1 1 0 1 0 1 1	00100000	0 0 1 0 0 0 0 0
wbv-cs--	1 1 1 0 1 1 0 0	00X00000	0 0 X 0 0 0 0 0
wbv-cs-t	1 1 1 0 1 1 0 1	01000000	0 1 0 0 0 0 0 0
wbv-csy-	1 1 1 0 1 1 1 0	0X000000	0 X 0 0 0 0 0 0
wbv-csyt	1 1 1 0 1 1 1 1	0XXXXXXX	0 X X X X X X X
wbvf----	1 1 1 1 0 0 0 0	10000000	1 0 0 0 0 0 0 0
wbvf---t	1 1 1 1 0 0 0 1	11111111	1 1 1 1 1 1 1 1
wbvf--y-	1 1 1 1 0 0 1 0	1XXXXXXX	1 X X X X X X X
wbvf--yt	1 1 1 1 0 0 1 1	XOXXXXXX	X 0 X X X X X X
wbvf-s--	1 1 1 1 0 1 0 0	X1XXXXXX	X 1 X X X X X X
wbvf-s-t	1 1 1 1 0 1 0 1	XXOXXXXX	X X 0 X X X X X
wbvf-sy-	1 1 1 1 0 1 1 0	XX1XXXXX	X X 1 X X X X X
wbvf-syt	1 1 1 1 0 1 1 1	XXXOXXXX	X X X 0 X X X X
wbvfc---	1 1 1 1 1 0 0 0	XXX1XXXX	X X X 1 X X X X
wbvfc--t	1 1 1 1 1 0 0 1	XXXXOXXX	X X X X 0 X X X
wbvfc-y-	1 1 1 1 1 0 1 0	XXXX1XXX	X X X X 1 X X X
wbvfc-yt	1 1 1 1 1 0 1 1	XXXXXOXX	X X X X X 0 X X
wbvfcs--	1 1 1 1 1 1 0 0	XXXXX1XX	X X X X X 1 X X
wbvfcs-t	1 1 1 1 1 1 0 1	XXXXXXOX	X X X X X X 0 X
wbvfcsy-	1 1 1 1 1 1 1 0	XXXXXX1X	X X X X X X 1 X
wbvfcsyt	1 1 1 1 1 1 1 1	XXXXXXX0	X X X X X X X 0
		XXXXXXX1	X X X X X X X 1
		XXXXXXXX	X X X X X X X X

Copying and Editing the Supplied Symbol Tables. You cannot directly edit any symbol tables supplied by the disassembler. But, you can make a copy of a supplied symbol table and then edit the copy for your specific use.

To create a new symbol table, follow these steps:

1. Select the Symbol Editor menu.
2. Press F2: FILE FUNCTIONS.
3. Select Open File in the Function field.
4. Select New File in the Edit Status field.
5. Enter a new symbol table file name.
6. Select Pattern or Range in the Table Type field to match the symbol table you are copying.
7. Press F5: EXECUTE FUNCTION.
8. Select Merge Files in the Function field.
9. Select the file to base your new symbol table on, such as the FB+_Stat file.
10. Press F5: EXECUTE FUNCTION.
11. Press F8: EXIT & SAVE.
12. Edit the file as desired. Refer to your *DAS 9200 System User Manual* for information on editing the symbol table.
13. Select the Channel menu.
14. Change the file name of the symbol table for the ST group (or whichever group's symbol table you are replacing) to the one that you specified in step 5.

TRIGGERING

All the Trigger menu selections available for use with your acquisition module are also available for use with disassembly. Refer to your module user manual for a list and description of these selections.

Unlike channel groups displayed with a numeric radix (such as hexadecimal), you cannot enter a numeric value in the word recognizer field for channel groups that are displayed symbolically. When you enter the name of a symbol, the corresponding value from the symbol table is used for triggering.

You can use the Home key to quickly clear the word recognizer field of any channel group with a symbolic radix, such as the ST group. To clear a word recognizer, open the field, press the Home key, and close the field. The first entry on the list is blank.

The Futurebus+ bus support product supplies a default trigger program for the FB_2-A96 and FB_3-A96 setups. Each default trigger program for these setups uses two internal DAS 9200 signals to allow the Main bus module and the Arb bus module to cross-trigger each other. The MainToArb signal is used for communication from the Main bus module to the Arb bus module. The ArbToMain signal is used for communication from the Arb bus module to the Main bus module.

The default trigger programs are set up to search for Main bus values that you enter in the word recognizer fields of the first trigger state in the Trigger menu of the Main bus module. When these values are found, or when the ArbToMain signal is received, the Main bus module sends the MainToArb signal to the Arb bus module, triggers, and stores data. The trigger program of the Arb bus module is set up likewise to check for a word recognizer match or to receive the MainToArb signal from the Main bus module, send the ArbToMain signal to the Main bus module, trigger, and store data.

Due to delays in intermodule signals, the trigger point in acquisition memory for the second module may be several samples behind the first module. Time correlation of the data from both modules, based on their timestamps, ensures an accurate representation of their relationship in time.

The DAS 9200 makes it possible to cross-trigger with other modules or to an external instrument. You may want to consider sending or receiving a signal to or from another module, or to the Sync Out SMB connector on the module. You should refer to your *DAS 9200 System User Manual* for an in-depth description of defining and using signals and to specific module user manuals for a description of using the Sync Out SMB connector.

Section 4: ACQUIRING AND VIEWING DISASSEMBLED DATA

This section describes how to acquire Main bus data and view it disassembled in the Disassembly display. This section explains:

- acquiring data
- viewing disassembled data
- functions of the Disassembly Format Definition overlay
- displaying groups symbolically
- restoring and viewing the demonstration reference memory
- searching through data
- printing data

ACQUIRING DATA

Once you load FBus+ or FBus64 support, or restore a supplied setup, choose a clocking mode, and specify the trigger, you are ready to acquire data. Press the F1: START acquisition key to begin the acquisition. You can press the F1: STOP key at any time to stop it.

If you have any problems acquiring data, refer to *Appendix A: Error Messages and Disassembly Problems*.

VIEWING DISASSEMBLED MAIN BUS DATA

To view disassembled Main bus data, press the Select Menu key, select the Main bus module, then select the Disasm menu, and press Return.

You should use the split-screen display to view Main bus and Arb bus data at the same time. Refer to your *92A96 Module User Manual* for information on how to use the split-screen display.

By default, the Disassembly display shows all acquired Futurebus+ transactions disassembled into individual beats. You can change the format of the Disassembly display (types of beats displayed, extent of information translation, and error display) in the Disassembly Format Definition overlay.

Figure 4-1 shows an example of the default Disassembly menu, and gives a brief description of the type of information disassembled and displayed. In this figure, all acquired beats are displayed. The discussion that follows describes the data displayed in the figure in greater detail.

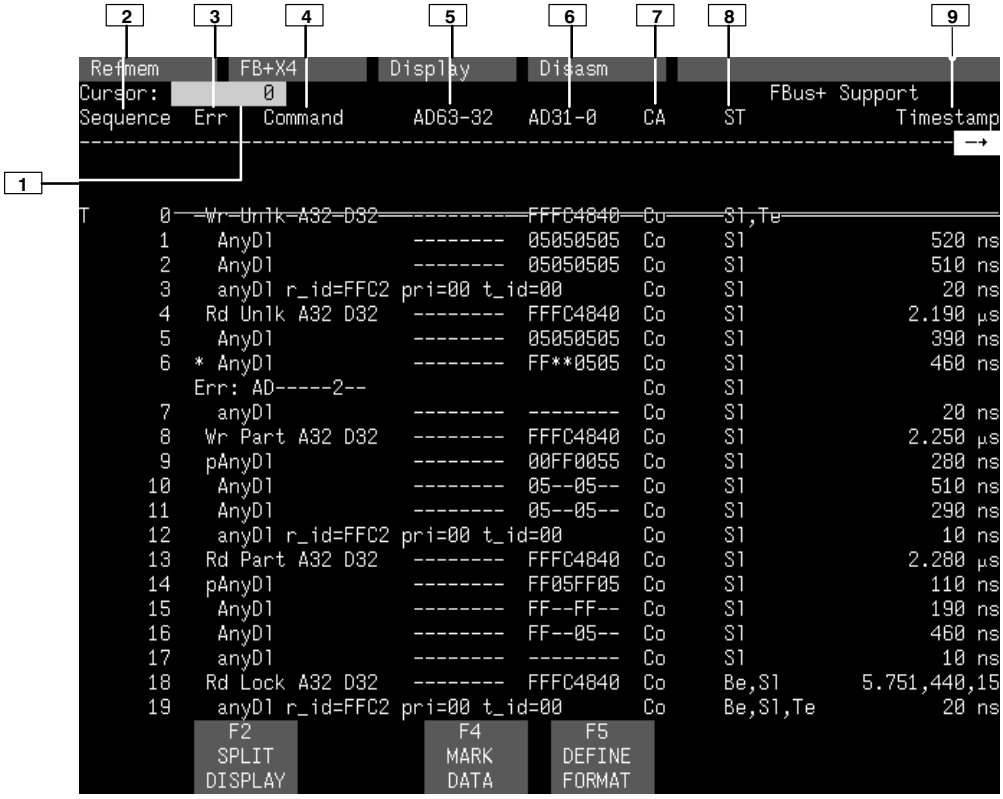


Figure 4-1. Default Disassembly menu.

1 **Cursor.** Shows the DAS 9200 sequence number on which the cursor is positioned.

2 **Sequence Column.** Lists DAS 9200 sequence numbers (memory locations) for the acquired data.

3 **Err Column.** Part of the mnemonic group; information is computed by the disassembler. An asterisk indicates that an error occurred in the acquired sample.

4 **Command Column.** Part of the mnemonic group; information is computed by the disassembler. The type of information will vary depending on the type of beat acquired.

5 **AD63-32 Column.** Part of the mnemonic group; information is computed by the disassembler.

6 **AD31-0 Column.** Part of the mnemonic group; information is computed by the disassembler.

7 **CA Group Column.** Lists data from channels corresponding to the Futurebus+ Capability signals. The default radix is symbolic.

8 **ST Group Column.** Lists data from channels corresponding to the Futurebus+ Status signals. The default radix is symbolic.

9 **Timestamp Column.** Lists the timestamp values when a timestamp selection is made in the Disassembly Format Definition overlay.

Gaps in the acquired data, caused by data qualification specified in the Trigger menu, are indicated by a gray background behind the AD63-32 and AD31-0 channel groups (not part of the mnemonic).

The sequence number identifies the DAS 9200 data sample. Each data sample of the Disassembly display represents one bus beat. An asterisk is displayed in the Err column if the disassembler has detected an error in the information for that bus beat.

Bus beat command information is displayed in the Command column. The disassembler displays AD (address/data) information in the AD63-32 and AD31-0 columns.

The disassembler displays the CA (capability) and ST (status) channel groups symbolically by default. All other channel groups are not displayed by default. Relative timestamp information (time elapsed from sample to sample) is also shown by default.

The disassembler computes the information in the Err, Command, AD63-32, and AD31-0 columns and displays it as one “mnemonic” group. Other bus information, such as for the CA and ST channel groups, is displayed as it is acquired (without any calculation by the disassembler), even if displayed symbolically.

The information in and the format of the mnemonic group is determined by the type of beat being disassembled: connect, data, or disconnect.

Beat Types. In Figure 4-1, the first bus transaction consists of four beats: a connect beat, two data beats, and a disconnect beat.

Command information for connect beats is not indented; Command information for data and disconnect beats is indented. This makes the connect beat (the beat that signals the start of a bus transaction) easier to identify.

For connect and data beats, the first letter of the Command information is uppercase. For disconnect beats, the first letter is lowercase.

The disassembler uses information from the Ph (phase) channel group (made up of signals generated by the probe adapter) to identify the type of bus beat being acquired.

Connect Beats. For each connect beat of a bus transaction, the disassembler displays translation of the bus CM information in the Command column, beginning with the transaction type. Figure 4-1 shows five types of transactions: Write Unlocked (sequence 0), Read Unlocked (sequence 4), Write Partial (sequence 8), Read Partial (sequence 13), and Read Locked (sequence 18). Table 4-1 describes all disassembled transaction types.

Table 4-1
Connect Beat Transaction Types

Label	Meaning	Label	Meaning
Rd Unlk	Read Unlocked	Wr Resp	Write Response
Wr Unlk	Write Unlocked	Rd Resp	Read Response
AO Unlk	Address Only Unlocked	WrNoAck	Write No Acknowledge
AOWUnlk	Address Only or Write Unlocked*	RdInval	Read Invalid
Rd Lock	Read Locked	WrInval	Write Invalid
Wr Lock	Write Locked	RdShare	Read Shared
AO Lock	Address Only Locked	CpyBack	Copyback
AOWLock	Address Only or Write Locked*	Rd Mod	Read Modified
Rd Part	Read Partial	Inval.	Invalidate
Wr Part	Write Partial	ShrResp	Shared Response
RdPrtLk	Read Partial Locked	ModResp	Modified Response
WrPrtLk	Write Partial Locked	RESERVD	-reserved-

*The actual transaction type is uncertain if the beat following the connect beat is not acquired.

The disassembler further decodes CM information and displays transaction address width (AW) and data width (DW) values for connect beats. Possible AW values are A32 and A64. Possible DW values are D32, D64, D128, and D256. You should keep in mind that while the CM value may specify a 256-bit transaction, the disassembler and probe adapter only support 128-bit wide data transfers.

Refer to Figure 4-1. Note that for sequence 0, dashes appear under the AD63-32 column for the connect beat because the transaction has specified a 32-bit address width. Address information for the transaction is displayed in hexadecimal in the AD31-0 column.

For some types of transactions, the AD lines do not carry address information in the connect beat. AD31-0 information is translated and the disassembler displays the hexadecimal value of the transaction requestor’s global identification as r_id, the requestor’s original transaction priority as pri, and the transaction identification as t_id. Figure 4-2 shows this at sequence 26.

Refer to Figure 4-1 again. Note that in sequence 0, CA information for the connect beat shows a compelled transaction. The status (ST) of the sequence shows it is selected, shown as Sl, and that there is a transaction error, shown as Te. Symbol tables for these channel groups can be found in Section 3.

Data Beats. CM information is first translated to display the data transfer length. Table 4-2 shows how data transfer information is displayed.

Table 4-2
Data Transfer Lengths

Data Transfer Length	Meaning
AnyDl	unrestricted data length
Dl=1	data length specification of 1
Dl=2	data length specification of 2
Dl=4	data length specification of 4
Dl=8	data length specification of 8
Dl=16	data length specification of 16
Dl=32	data length specification of 32
Dl=64	data length specification of 64

The disassembler may display additional information in the CM column. Table 4-3 shows the type of information that could be displayed for compelled data beats of locked transactions.

Table 4-3
Locked Commands

Data Transfer Length	Meaning
NoLOCK	-No command-
MskSwp	Mask and swap
CmpSwp	Compare and swap
FetAdB	Fetch and add big
FetAdL	Fetch and add little
RESERV	-Reserved-

Other information may also be displayed, such as Sw for slave write. For data beats of packet transactions, the disassembler can also display an Lt for last transaction, and Pr for packet request. Figure 4-7 shows this at sequence 2.

Refer to Figure 4-1. Note that for sequences 1 and 2, dashes appear under the AD63-32 column for the data beats because the transaction has specified a 32-bit address width. Address information for the transaction is displayed in hexadecimal in the AD31-0 column.

Sequence 6 in Figure 4-1 shows an asterisk in the Err column. This indicates that the disassembler found an error in that data beat of the Read Unlock transaction. Asterisks in the AD31-0 column indicate a parity error in AD23-16. A description of all errors (default in the Disassembly Format Definition overlay) displays on the line following the beat with the error. In this example, the only error found was a parity error in byte 2 of the AD31-0 lines. Information for the other groups (such as CA and ST) is also repeated in the error line. Table 4-4 shows all additional information that can be displayed in the error line.

The transaction at sequences 8 through 12 show a Write Partial in which the first data beat communicates Byte Lane Deselect information for use in transferring data during the following data beats. A “p” to the left of the Data Transfer Length specification emphasizes that this is a Partial Lane Deselect data beat.

Because the data width specified in the connect beat was 32-bits, only the lower four bits of the Lone Deselect value shown in the AD31-0 column are meaningful. In sequence 9, the value of AD3-AD0 is 5 (hexadecimal), which means that bytes 0 and 2 of the remaining data beats will not be transferring valid data. Sequences 10 and 11 show dashes in those byte positions.

Disconnect Beats. The last beat of the first transaction shown in Figure 4-1 (sequence 3) is the disconnect beat. The disassembler displays Data Transfer Length information for disconnect beats like it displays Data Transfer Length information for data beats. Table 4-2 shows Data Transfer Length information.

Unlike data beats, the first letter of a disconnect beat is always displayed as lowercase. An sw for slave write, an mr for more, and an lk for lock may also be displayed. Figure 4-8 shows this at sequence 0.

Refer to Figure 4-1, sequence 3. Because the transaction was a write, information is communicated on AD31-0 during the disconnect beat. The information is translated and the disassembler displays the hexadecimal value of the transaction requestor’s global identification as r_id, the requestor’s original transaction priority as pri, and the transaction identification as t_id.

The disassembler may also display an sl for selected (from AD2), bs for busy (from AD1), or te for transaction error (from AD0).

Timestamps. Timestamps for connect and data beats show the time relative to the start of the acquisition when the probe adapter signaled the DAS 9200 that a particular bus beat ended. Logic circuitry on the probe adapter examines the edges of the AS* and DS* bus handshake signals to know when these types of beats end.

Timestamps for disconnect beats are about 20 ns later than the previous beat of the transaction. (Logic circuitry on the probe adapter causes the DAS 9200 to record disconnect beat information about 20 ns after recording information for the previous beat.) Because the timestamp counter changes in 10 ns increments, relative timestamps for disconnect beats can be displayed as 30 ns or 10 ns. Figure 4-1 shows this at sequences 12 and 17.

Other Displayed Information. Figure 4-2 shows the same acquired data as in Figure 4-1; the Ph (phase), AD31-0, and BP7-0 channel groups have been added to the display menu through the Disassembly Format Definition overlay. With the Ph group shown symbolically, a symbol for the type of beat is displayed for each sequence. Information displayed in the second AD31-0 column is for the AD31-0 channel group; it shows the actual AD31-AD0 bus information as acquired. (Remember that the disassembler calculates the AD31-0 information shown in the first AD31-0 column portion of the mnemonic group.)

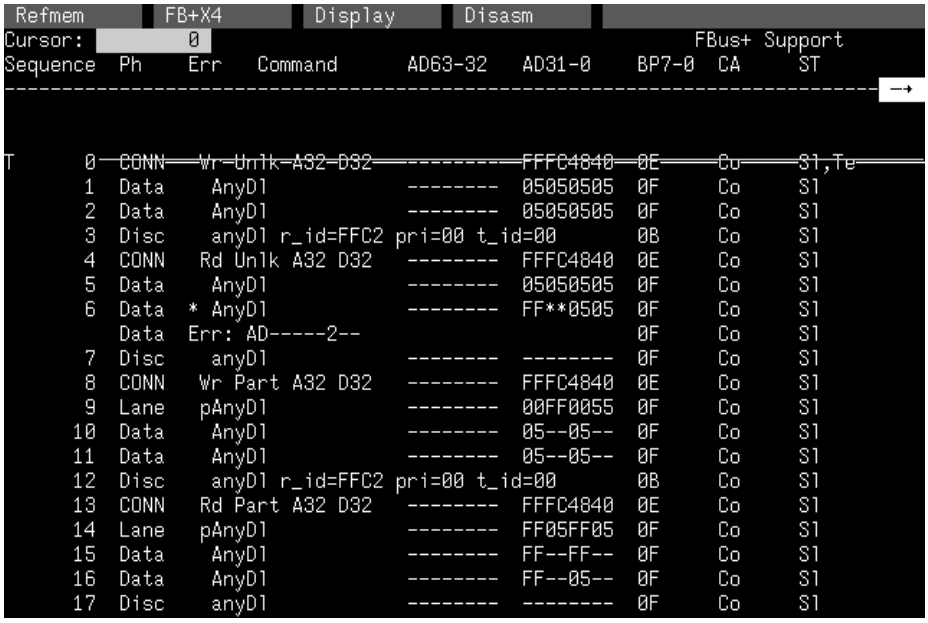
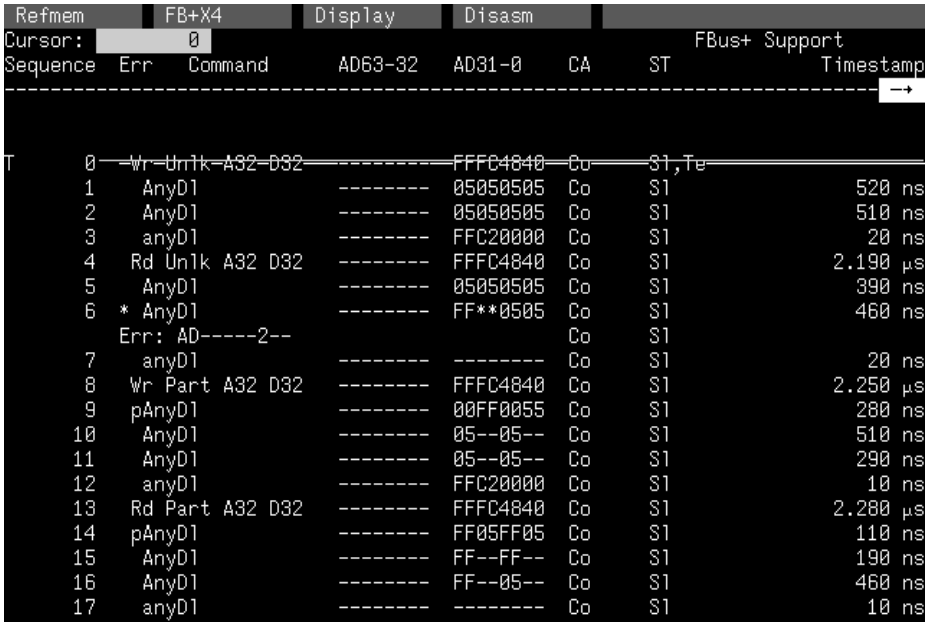


Figure 4-2. Disassembly menu with Ph, AD31-0, and BP7-0 channel group values.

Another way to clarify the Ph, CM, and AD values (and more convenient than adding additional groups to the display) is to change the way the information is translated through a selection in the Disassembly Format Definition overlay. Figure 4-3 shows the same acquired data as in Figure 4-1 but without translated AD information.

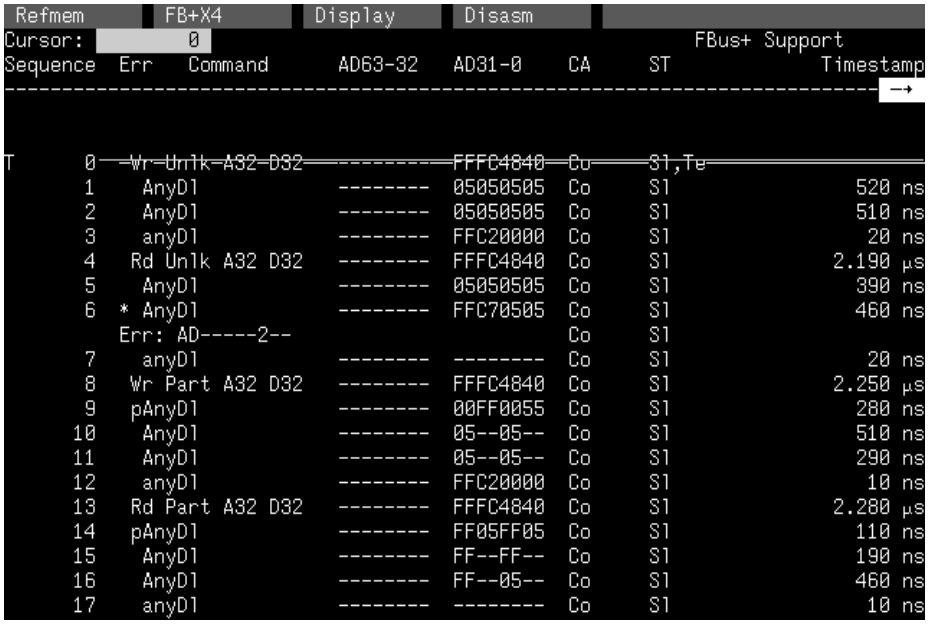


```
Refmem    FB+X4    Display    Disasm
Cursor:       0                                          FBus+ Support
Sequence  Err   Command      AD63-32   AD31-0    CA    ST            Timestamp
-------------------------------------------------------------------------------→

T      0  -Wr-Unlk-A32-D32-----------FFFC4840--Co----S1,Te-------------------
       1    AnyDl             --------  05050505  Co    S1              520 ns
       2    AnyDl             --------  05050505  Co    S1              510 ns
       3    anyDl             --------  FFC20000  Co    S1               20 ns
       4   Rd Unlk A32 D32    --------  FFFC4840  Co    S1            2.190 µs
       5    AnyDl             --------  05050505  Co    S1              390 ns
       6  * AnyDl             --------  FF**0505  Co    S1              460 ns
          Err: AD-----2--                          Co    S1
       7    anyDl             --------  --------  Co    S1               20 ns
       8   Wr Part A32 D32    --------  FFFC4840  Co    S1            2.250 µs
       9   pAnyDl             --------  00FF0055  Co    S1              280 ns
      10    AnyDl             --------  05--05--  Co    S1              510 ns
      11    AnyDl             --------  05--05--  Co    S1              290 ns
      12    anyDl             --------  FFC20000  Co    S1               10 ns
      13   Rd Part A32 D32    --------  FFFC4840  Co    S1            2.280 µs
      14   pAnyDl             --------  FF05FF05  Co    S1              110 ns
      15    AnyDl             --------  FF--FF--  Co    S1              190 ns
      16    AnyDl             --------  FF--05--  Co    S1              460 ns
      17    anyDl             --------  --------  Co    S1               10 ns
```

Figure 4-3. Disassembly menu with only CM information translated.

Figure 4-4 shows the same acquired data as in Figure 4-3 without displaying asterisks for AD bytes with parity errors.

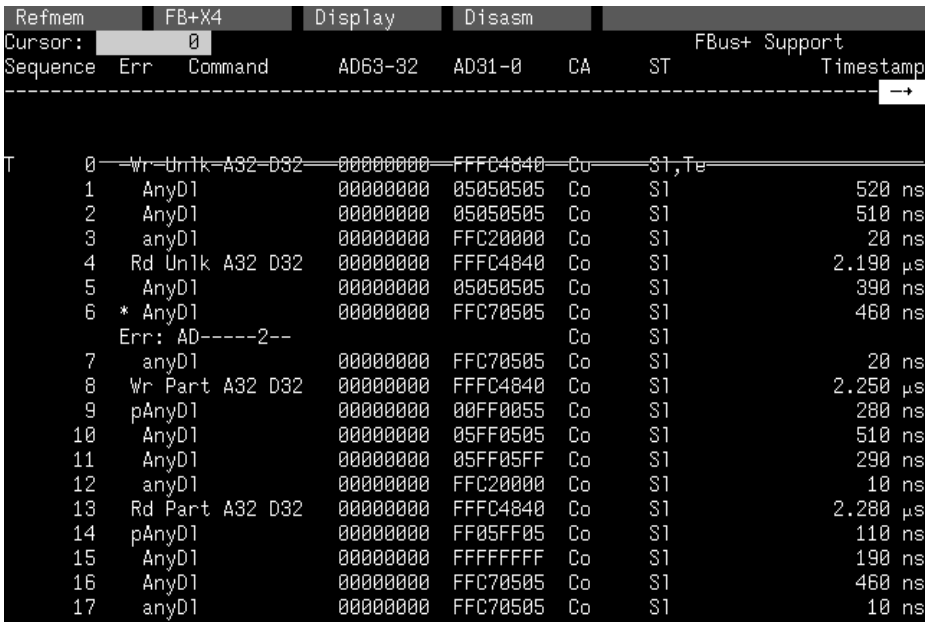


```
Refmem    FB+X4    Display    Disasm
Cursor:       0                                          FBus+ Support
Sequence  Err   Command      AD63-32   AD31-0    CA    ST            Timestamp
-------------------------------------------------------------------------------→

T      0  -Wr-Unlk-A32-D32-----------FFFC4840--Co----S1,Te-------------------
       1    AnyDl             --------  05050505  Co    S1              520 ns
       2    AnyDl             --------  05050505  Co    S1              510 ns
       3    anyDl             --------  FFC20000  Co    S1               20 ns
       4   Rd Unlk A32 D32    --------  FFFC4840  Co    S1            2.190 µs
       5    AnyDl             --------  05050505  Co    S1              390 ns
       6  * AnyDl             --------  FFC70505  Co    S1              460 ns
          Err: AD-----2--                          Co    S1
       7    anyDl             --------  --------  Co    S1               20 ns
       8   Wr Part A32 D32    --------  FFFC4840  Co    S1            2.250 µs
       9   pAnyDl             --------  00FF0055  Co    S1              280 ns
      10    AnyDl             --------  05--05--  Co    S1              510 ns
      11    AnyDl             --------  05--05--  Co    S1              290 ns
      12    anyDl             --------  FFC20000  Co    S1               10 ns
      13   Rd Part A32 D32    --------  FFFC4840  Co    S1            2.280 µs
      14   pAnyDl             --------  FF05FF05  Co    S1              110 ns
      15    AnyDl             --------  FF--FF--  Co    S1              190 ns
      16    AnyDl             --------  FF--05--  Co    S1              460 ns
      17    anyDl             --------  --------  Co    S1               10 ns
```

Figure 4-4. Disassembly menu without asterisks to indicate AD bytes with parity errors.

Figure 4-5 shows the same acquired data as in Figure 4-4 without displaying dashes for invalid AD bytes.

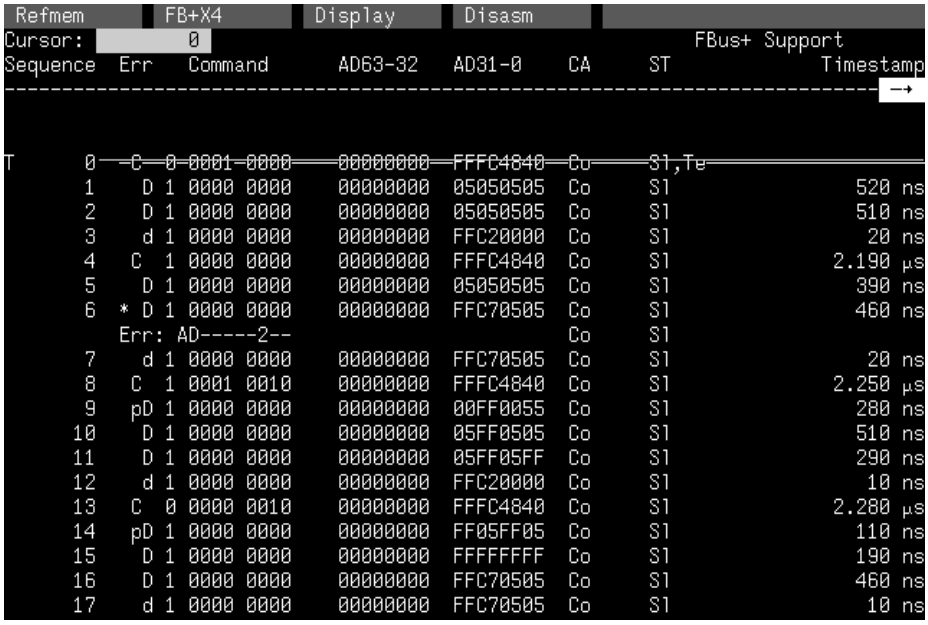


```
Refmem   FB+X4   Display   Disasm
Cursor:      0                                          FBus+ Support
Sequence  Err   Command      AD63-32   AD31-0    CA     ST            Timestamp
-------------------------------------------------------------------------------→

T      0  -Wr Unlk A32 D32   00000000  FFFC4840  Co     S1,Te
       1    AnyDl            00000000  05050505  Co     S1              520 ns
       2    AnyDl            00000000  05050505  Co     S1              510 ns
       3    anyDl            00000000  FFC20000  Co     S1               20 ns
       4   Rd Unlk A32 D32   00000000  FFFC4840  Co     S1            2.190 µs
       5    AnyDl            00000000  05050505  Co     S1              390 ns
       6  * AnyDl            00000000  FFC70505  Co     S1              460 ns
          Err: AD-----2--                         Co     S1
       7    anyDl            00000000  FFC70505  Co     S1               20 ns
       8   Wr Part A32 D32   00000000  FFFC4840  Co     S1            2.250 µs
       9   pAnyDl            00000000  00FF0055  Co     S1              280 ns
      10    AnyDl            00000000  05FF0505  Co     S1              510 ns
      11    AnyDl            00000000  05FF05FF  Co     S1              290 ns
      12    anyDl            00000000  FFC20000  Co     S1               10 ns
      13   Rd Part A32 D32   00000000  FFFC4840  Co     S1            2.280 µs
      14   pAnyDl            00000000  FF05FF05  Co     S1              110 ns
      15    AnyDl            00000000  FFFFFFFF  Co     S1              190 ns
      16    AnyDl            00000000  FFC70505  Co     S1              460 ns
      17    anyDl            00000000  FFC70505  Co     S1               10 ns
```

Figure 4-5. Disassembly menu without dashes to indicate invalid AD bytes.

Figure 4-6 shows the same acquired data as in Figure 4-5 without translation of CM or AD information. The CM value is displayed in binary and the Ph group is displayed symbolically (C for connect beats, pD for partial lane deselect data beats, D for data beats, and d for disconnect beats).



```
Refmem   FB+X4   Display   Disasm
Cursor:      0                                          FBus+ Support
Sequence  Err   Command      AD63-32   AD31-0    CA     ST            Timestamp
-------------------------------------------------------------------------------→

T      0  -C  0-0001-0000    00000000  FFFC4840  Co     S1,Te
       1    D 1 0000 0000    00000000  05050505  Co     S1              520 ns
       2    D 1 0000 0000    00000000  05050505  Co     S1              510 ns
       3    d 1 0000 0000    00000000  FFC20000  Co     S1               20 ns
       4   C  1 0000 0000    00000000  FFFC4840  Co     S1            2.190 µs
       5    D 1 0000 0000    00000000  05050505  Co     S1              390 ns
       6  * D 1 0000 0000    00000000  FFC70505  Co     S1              460 ns
          Err: AD-----2--                         Co     S1
       7    d 1 0000 0000    00000000  FFC70505  Co     S1               20 ns
       8   C  1 0001 0010    00000000  FFFC4840  Co     S1            2.250 µs
       9   pD 1 0000 0000    00000000  00FF0055  Co     S1              280 ns
      10    D 1 0000 0000    00000000  05FF0505  Co     S1              510 ns
      11    D 1 0000 0000    00000000  05FF05FF  Co     S1              290 ns
      12    d 1 0000 0000    00000000  FFC20000  Co     S1               10 ns
      13   C  0 0000 0010    00000000  FFFC4840  Co     S1            2.280 µs
      14   pD 1 0000 0000    00000000  FF05FF05  Co     S1              110 ns
      15    D 1 0000 0000    00000000  FFFFFFFF  Co     S1              190 ns
      16    D 1 0000 0000    00000000  FFC70505  Co     S1              460 ns
      17    d 1 0000 0000    00000000  FFC70505  Co     S1               10 ns
```

Figure 4-6. Disassembly menu without translating CM or AD information.

Figure 4-7 shows the same acquired data as in Figure 4-1 with only connect beats displayed.

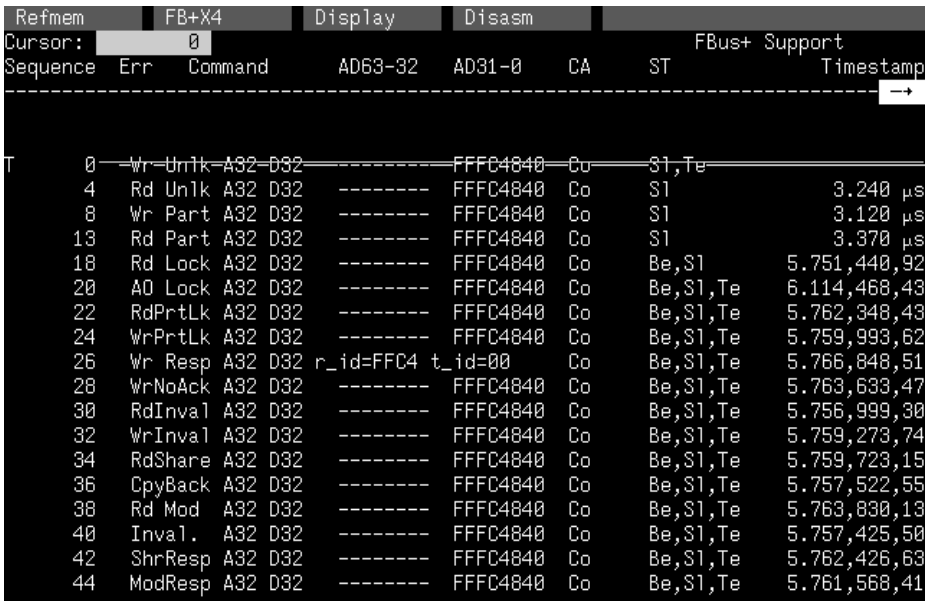


Figure 4-7. Disassembly menu with only connect beats displayed.

Figure 4-8 shows additional CM information that could be displayed in the various types of beats. This is not the same acquired data as shown in Figures 4-1 through 4-7 and is not typical of normal Futurebus+ activity. In this figure, CM information in sequence 0 (also in sequences 3, 6, 7, 8, 9 , and 11) contains a parity error. The display line shows periods in the Command column to indicate this.

Sequence 0 is the first acquired sample and is a disconnect beat, indicated by the lowercase dl; dl is the Data Transfer Length specification. Since information from the connect beat of the transaction is missing (was not acquired), the error line shows an Uncertain context error (Un). This means that the display for beats of that transaction may be wrong because there was no connect beat information available.

Figure 4-8 also shows the various formats of the symbols for the ST channel group. The disassembler displays a two-letter abbreviation for all asserted bits, separated by commas whenever there is enough space on the display to do so. As more bits are asserted, the commas will not be displayed. As even more bits are asserted, only one-letter abbreviations are displayed with dashes for any unasserted bits. Refer to Section 3 to see the symbol table for the ST group.

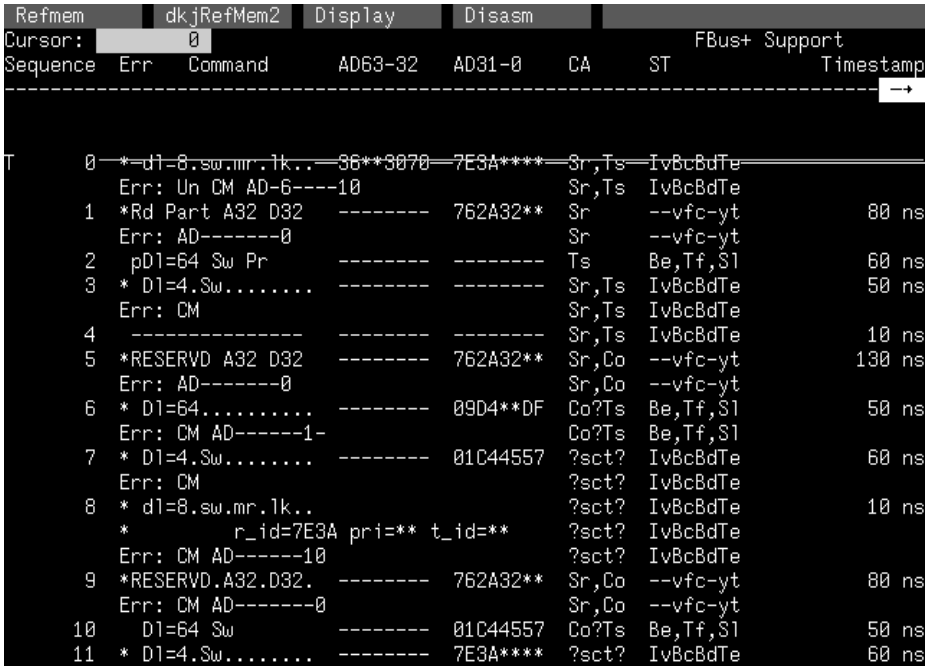


Figure 4-8. Disassembly menu with ST symbols showing their various formats.

Sequence 4 shows dashes for the CM information. This only occurs for the disconnect beat of a packet read transaction.

The CA symbols for sequences 6 through 8 show question marks to indicate that the value is unusual. Refer to Section 3 to see the symbol table for the CA group.

Sequence 8 also contains more disassembled information than can fit on one line. AD translation is displayed on a second line with an extra line containing error reporting information following that. In this example, the low two bytes of AD31-0 contain parity errors, as shown by the two asterisks (**) following the pri and t_id indicators. In transactions where the low byte of AD31-0 is translated to show sl, bs, or te indicators, a parity error is shown with a question mark appended to the indicator, such as sl?, bs?, or te?.

If you have set the clocking option in the Clock menu to acquire Power Up Cycles, and the POWERED signal (in the Ph channel group) is not asserted in the acquired sample, the disassembler displays the following line below the affected sample:

^Warning: Power up/down cycle!

Note that this is not considered an error; an asterisk is not displayed in the Err column. Figure 4-9 shows this line displayed at sequences 3880 and 3881.

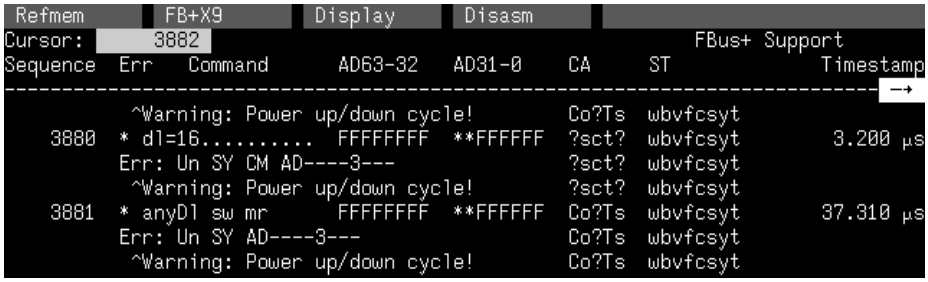


Figure 4-9. Display of Power Up cycles.

Error Reporting

If the Error Reporting field is set to Extra Line in the Disassembly Format Definition overlay, a description of all errors present displays on the line following the beat with the error. Table 4-4 shows the possible character combinations displayed in the error line and their meaning.

Table 4-4
Extra Error Line Information

Display Characters	Meaning
Un	Uncertain context (connect beat information for the transaction is unavailable
Sy	Synchronization error (sequence of beats is invalid)
CM	CM parity error
TG	TG parity error
AD	AD parity error*
D	D parity error*
*For example: AD-6----10 signals three parity errors in bytes 6, 1, and 0.	

Disassembly Format Definition Overlay

The Disassembly Format Definition overlay allows you to make optional display selections for the Disassembly menu and tailor it for your applications. To access this overlay, press F5: DEFINE FORMAT.

You can use this overlay to do the following:

- specify which beats are displayed
- set the interval in which the data cursor will scroll through disassembled data
- display and define the format of the timestamp
- highlight various types of beats

- change the position of any channel group in the display
- change the radix for any channel group
- choose which symbol tables are used when channel groups are displayed symbolically

The names of the selections in three fields of the overlay are carried over from microprocessor disassembly support and have no logical meaning for the Futurebus+ bus support. These fields are the Display Mode, Scroll By, and Highlight fields.

Table 4-5 shows the name of the selection as it appears for each of these three fields, and the beat-select function of that selection for the Futurebus+ disassembler.

Table 4-5
Display Mode, Scroll By, and Highlight Fields and Beat-Select Functions

Selection Name by Field			Beat-Select Function
Display Mode	**Scroll By**	**Highlight**	
Hardware (default)	Sequence (default)	All	All beats without regard to the selection in the Qualification field
Software	Instruction	Instructions (default)	All beats as determined by the selection in the Qualification field
Control Flow	Control Flow	Control Flow	Connect and disconnect beats as determined by the selection in the Qualification field
Subroutine	Subroutine	Subroutines	Only connect beats as determined by the selection in the Qualification field

Figure 4-10 shows the Disassembly Format Definition overlay.

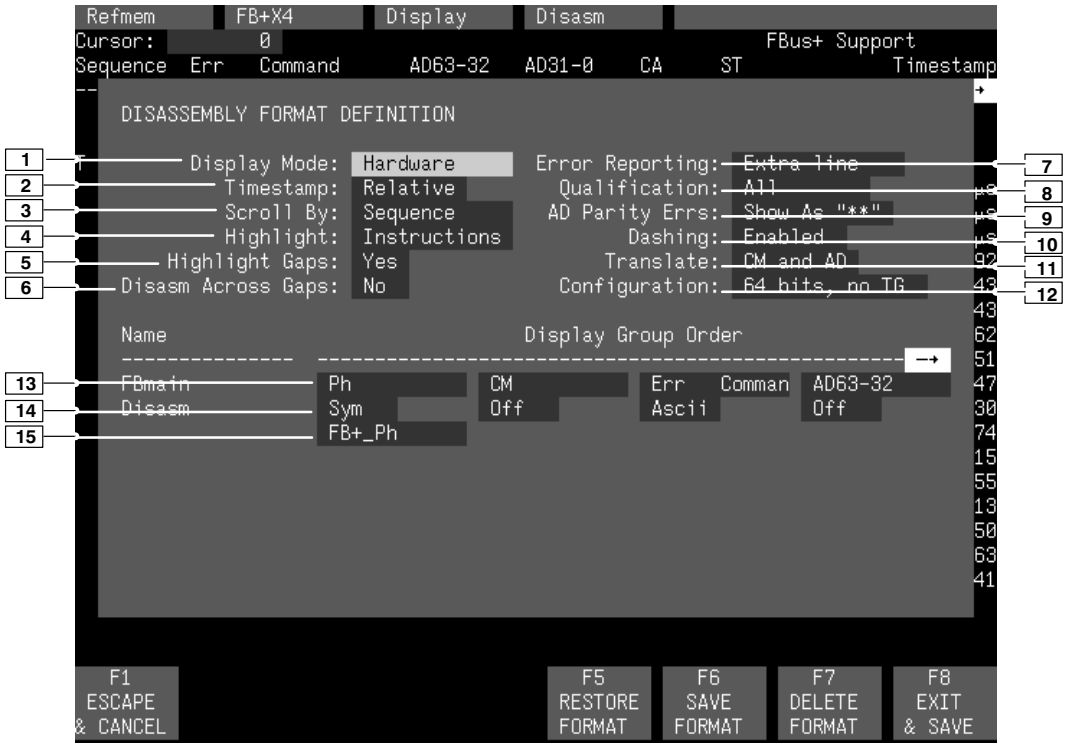


Figure 4-10. Disassembly Format Definition overlay.

1 **Display Mode.** You can display disassembled beats according to selections defined in Table 4-5.

2 **Timestamp.** You can display the timestamp as an Absolute, Relative, or Delta value. You can also set the timestamp display to Off. Refer to the description of timestamps earlier in this section for more information about timestamps for disconnect beats.

Timestamp values show the amount of time that has elapsed between data samples. An Absolute timestamp shows the amount of time elapsed between when the acquisition was started (after pressing F1: START) and each subsequent data sample. A Relative timestamp shows the amount of time elapsed between successive samples. A Delta timestamp shows the amount of time between the sample with the delta user mark and each previous or subsequent data samples.

3 **Scroll By.** You can scroll by disassembled beats according to selections defined in Table 4-5.

4 **Highlight.** You can highlight disassembled beats according to selection defined in Table 4-5.

With highlighting on, only the selected type of samples are shown as white text with a black background; all other samples are shown as gray text with a black background.

5 **Highlight Gaps.** You can choose to highlight or not to highlight gaps. Gaps are caused by qualifying data storage in the Trigger menu of either the Main bus or the Arb bus module and are indicated by a gray background behind the AD64-32 and AD31-0 values.

6 **Disasm Across Gaps.** You can choose to continue or not to continue to disassemble data across gaps. Disassembling data across gaps causes the disassembler to disassemble data as if no gap existed. Disassembled data will be invalid if the last sample before the gap does not logically match the sample immediately following the gap.

For example, with the Trigger menu set up to cause certain data beats to not be acquired, disassembly across gaps would not be a problem. In fact, not disassembling across gaps would result in erroneous error reporting.

7 **Error Reporting.** You can display an extra line beneath a beat containing an error that provides more information about the error. Refer to the general description of the Disassembly menu earlier in this section for descriptions of the type of information that may be displayed. More information can also be found under the description of *Error Reporting* earlier in this section.

8 **Qualification.** You can qualify which beats are displayed, scrolled to, and highlighted. You can select All beats, Errors (beats with errors), or Non-Errors (beats without errors).

The combination of selections made in the Display Mode field and the Qualification field can affect the data being displayed. This can also cause no display of information.

9 **AD Parity Bits.** You can display parity errors as asterisks on a byte-by-byte basis in the AD63-32 and AD31-0 channel groups with the Shown as “**” selection. The Shown As Is selection displays the actual data instead.

10 **Dashing.** You can enable or disable the display of invalid data (such as data bytes without meaningful value) as dashes in the AD63-32, AD31-0, D127-D96, and D95-64 channel groups. The Disabled selection displays the actual data instead.

Data bytes that would be dashed under Enabled can never have parity errors.

11 **Translate.** You can specify which groups of the mnemonic are translated or shown without translation. The default selection translates data for the CM and AD31-0 groups. Other selections are CM Only, AD Only, and Off (no translation).

When CM translation is enabled, transaction type and other information is decoded from the CM values and displayed. When AD translation is enabled, the value of the AD31-0 group is displayed using mnemonics for connect or disconnect beats of certain types of transactions in which AD31-0 is used to communicate information other than address information.

12 **Configuration.** You can configure the disassembler to check for parity errors on AD63-32, D127-96, D95-64, and TG depending upon the configuration selected here. If you choose the 32-bit wide data bus, the computed mnemonic group displays blanks in the AD63-32 column. The format of the AD parity error reporting on the extra error line (if selected) will only display four data bytes.

The default selection is 64-bits, No TG. To acquire data from a 128-bit wide bus, you must also change the radix for the D127-D96 and D95-D64 channel groups from Off to Hex.

13 **Group Name.** You can specify the name of the group that displays in the column in which the cursor is positioned. When you move a group, the group is inserted in the new column position and removed from its old position. All the groups to the right of the inserted group are moved over one column position to the right.

14 **Group Radix.** You can select the radix in which each group displays. The radix selections for most groups are Binary, Octal, Hexadecimal, Symbol, and Off. You should only select the symbolic radix when a symbol table is available for that group. The timestamp value always displays in decimal.

The only selections for the mnemonic group (Err Comman) are ASCII or Off.

15 **Symbol Table.** You can specify a symbol table to use for each group when symbolic is the selected radix.

Function Keys

F1: ESCAPE & CANCEL. Closes the overlay and discards any changes you have made since entering it.

F5: RESTORE FORMAT. Displays a list of saved disassembly formats for the current module or cluster setup. Use the cursor keys to select the desired format to restore and press the Open/Close key.

F6: SAVE FORMAT. Saves the current selections for the Disassembly Format Definition overlay in a file on disk. You can enter a file name up to ten characters long.

F7: DELETE FORMAT. Displays a list of saved disassembly format files for the current module or cluster setup. Use the cursor keys to select the desired format to delete and press the Open/Close key. You cannot delete the Default format.

F8: EXIT & SAVE. Exits the overlay and executes or saves any changes made.

Displaying Off-Screen Channel Groups

When the number of channel groups to display exceeds the amount of screen space, arrows (▶) show on the right side of the screen. The arrows indicate that there are channel groups turned on in the Disassembly Format Definition overlay, but there is not enough room to display them. To display a hidden group, do the following:

1. Press F5: DEFINE FORMAT from the Disassembly menu.
2. Place the cursor in the first channel group field under the Display Group Order part of the overlay.
3. Press the Return key to display the channel group selections, select the group you want displayed, and press Return again.

To turn off a channel group (that is, remove it from the display), do the following:

1. Press F5: DEFINE FORMAT from the Disassembly menu.
2. Move the cursor to the channel group that you would like to remove from the display and select OFF as the radix.

NOTE

Do not turn off the Err Comman group. If you turn off the Err Comman group, disassembled data will no longer appear.

3. Press F8: EXIT & SAVE.

Displaying Channel Groups Symbolically

All channel groups can be displayed as symbolic values in the Disassembly display similar to the way the Ph, CA, and ST groups can be displayed as symbol values in the Disassembly menu. You can use the Symbol Editor menu to create symbol tables in which symbols are assigned to various ranges or patterns. You can then change the radix of the channel group to symbolic in the Disassembly display using the Disassembly Format Definition overlay.

You should be aware that the disassembler computes the information that displays under the Err, Command, AD63-32, and AD31-0 column headings. Information shown in this mnemonic group is not the same as and should not be confused with the actual 92A96 channel groups. For example, the AD63-32 and AD31-0 display of the mnemonic group is not the same as the actual AD63-32 and AD31-0 channel groups. If you select symbolic radix and a symbol table for the AD63-32 or AD31-0 channel groups, they will appear (by default) next to the AD63-32 and AD31-0 information of the mnemonic group.

SEARCHING THROUGH DATA

The disassembler does not have a Disassembly Search Definition overlay. However, you can effectively search through disassembled data by following these steps:

1. Press F2: SPLIT DISPLAY to use the split-screen display.
2. Press F5: SPLIT HORIZ to split the screen into two horizontal displays.
3. Press F2: LOCK CURSOR. A list of selections appears.
4. Select **lock cursors at the same sequence** and press Return.
5. Press F8: EXIT & SAVE to display the menus in a split screen.
6. If the active window is the Disassembly menu, press F3: SWITCH WINDOWS to make the State menu active. The cursor and Cursor field are yellow in the active window.
7. Press F6: DEFINE SEARCH to use the search function of the State menu to search for the desired sequence.

To search on Ph, CA, or ST group values, change the radix to binary and refer to Tables 3-2, 3-3, or 3-5 to find the binary equivalent values for the cycles you want to locate.

When searching for data in a clustered module setup in the State menu, the searches are conducted only for the master module. You can, however, define either module to be the master module. Refer to the description of the State Search Definition overlay in your *92A96 Module User Manual* for a description of how to search through state data. Also refer to that manual for a description of how to return to a full-screen display.

To abort a search, press the Esc (escape) key.

Figure 4-11 shows the screen split into Disassembly and State windows with the cursors locked on the same bus cycle.

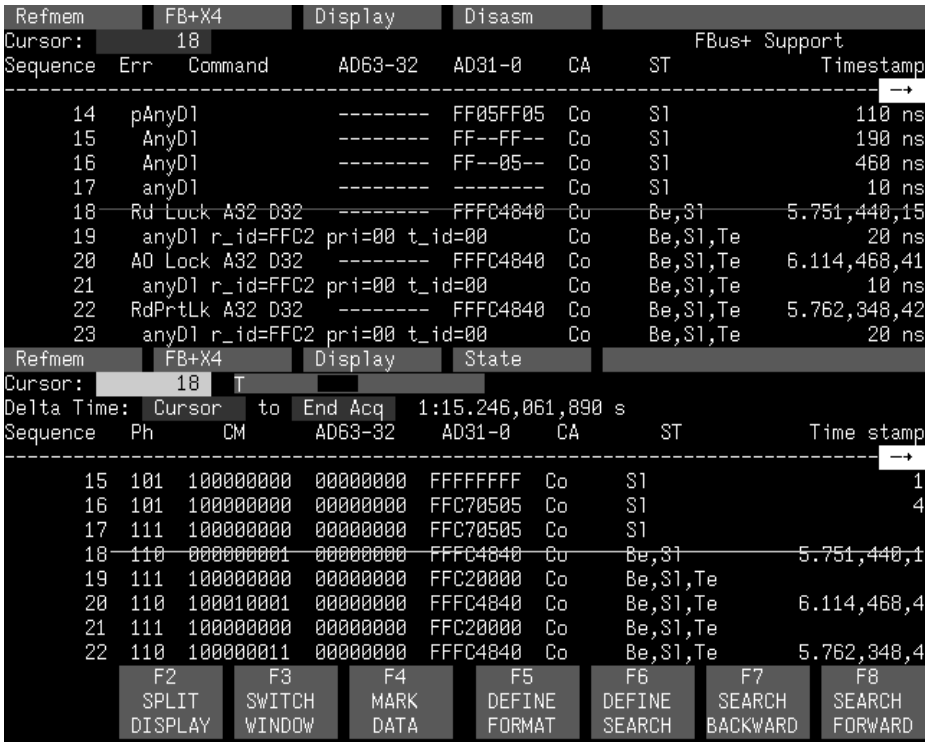


Figure 4-11. Disassembly and State split-screen display. You can use this method to perform searches.

PRINTING DATA

To print disassembled data, use the Disassembly Print overlay. To access this overlay, press the Shift and Print keys at the same time from the Disassembly menu. The Disassembly Print overlay is exactly the same as the State Table Print overlay. Refer to your *92A96 Module User Manual* for a description of this overlay.

REFERENCE MEMORY

A demonstration reference memory file is provided so you can see the way the Futurebus+ mnemonics look when they are disassembled. In this discussion, you will view the reference memory. Viewing the reference memory is not a requirement for preparing the 92A96 Module for use. You can view the reference memory file without connecting the DAS 9200 to your SUT.

To view the FB+_Demo Refmem, follow these steps:

1. Press the Select Menu key and select the FB+_Demo file from the Refmem column.
2. Select the Disasm menu and press Return.

You can affect the display of the disassembled data from the Disassembly Format Definition overlay, which you can access through the Disassembly menu. Displaying all disassembled beats is the default format.

If there is not enough free space on the hard disk, you can delete the FB+_Demo file. It is not necessary to the operation of the disassembler.

Section 5: GENERAL PURPOSE ANALYSIS

You may need to perform general purpose (timing) analysis on your Futurebus+ system prior to, during, and after attempting to integrate your software with the Futurebus+ system hardware. When performing hardware analysis, you will want to use the data acquisition module to acquire data with a finer resolution. When more data samples are taken in a given period of time, the resolution in the Timing display increases, letting you see signal activity that would otherwise go undetected.

This section provides information on the following:

- clocking
- triggering
- displaying data
- supplied Timing Format Definition files

To acquire and display timing data, you need to change the clocking selection and trigger program, acquire data, and view it in the Timing menu. Three predefined Timing Format Definition overlay files called Fbus+_96, Fbus+Arb_96, and FB_Arb_96 can be used to view Futurebus+ timing data. A description of these files and how to use them can be found later in this section.

Keep in mind when you view data in the State display that it uses the default channel grouping setup with all groups visible and will look very different than the Disassembly display.

There often is a need to view data in a split screen display with state data in one half and timing data in the other. Do not disconnect any of the 92A96 probe cables or interface housings if you are analyzing data in this manner. Instead, use channels available for alternate connections to make other Futurebus+ system connections. Refer to the channel assignment tables in Appendix C for information about channels not used for disassembly that are available for alternate connections.

CLOCKING

To change the data sampling rate, use the Clock menu.

The Sync/Async switch for the Main bus (S1) or Arb bus (S2) must be in the Async position to acquire timing data. The switches can be set independently of each other. For example, S1 can be set to Sync for synchronous acquisition of the Main bus and S2 can be set to Async for asynchronous acquisition of the Arb bus. For more information on the Sync/Async switches, refer to Section 2.

When using the 92A96 Module for timing analysis, you will want to use the Internal or External clocking modes. The Internal clock selection can sample data up to 100 MHz, which has a 10 ns resolution between samples. The External clock selection samples data on every active clock edge on the 92A96 clock inputs up to 100 MHz.

The Clock menu is shown in Figures 3-2 and 3-3. The default clocking mode is Custom when Main bus support is used; you will need to change it to either Internal or External. Your *92A96 Module User Manual* contains an in-depth description of Internal and External clocking.

Custom Clocking

Custom clocking only stores one data sample for each beat of the bus transaction. This clocking selection is generally unproductive for timing analysis. Refer to Appendix B for a more in-depth description of how Custom clocking acquires data.

Internal Clocking

When you select Internal as the clocking mode, the data acquisition module stores one data sample as often as every 10 ns (100 MHz). This clocking selection is commonly referred to as asynchronous.

Two typical uses of Internal clocking might be to verify that all the Futurebus+ signals are transitioning as expected or to measure timing relationship between signals.

It is possible to acquire asynchronous data at rates of 200 MHz and 400 MHz. The faster the 92A96 Module acquires data, the fewer channels it can acquire data on. A single 92A96 Module can acquire data on 24 channels at 400 MHz or 2.5 ns resolution. Refer to your *92A96 Module User Manual* for information on sampling data at speeds faster than 100 MHz.

External Clocking

When you select External as the clocking mode, the data acquisition module acquires and stores data based on the clock channel up to 100 MHz. This clocking selection is commonly referred to as synchronous.

By selecting the rising edge of CLK:0 on the data acquisition module as the clock channel, and turning off the remaining three clocks, the data acquisition module will sample data on every rising edge of the clock.

No data is acquired on the falling clock edge unless you select both edges.

You can also use the other three clock channels as qualifiers or clocks to further modify the clocking in of data from your Futurebus+ system.

TRIGGERING

All the Trigger menu selections currently available for your data acquisition module are still valid for timing analysis. Refer to your module user manual for a list and description of the selections.

ACQUIRING DATA

You can acquire data as described in the *Acquiring Data* description in Section 4.

DISPLAYING DATA

Timing analysis requires that you view data in either the State or Timing menus. The following discussion describes these menus.

Timing Menu

In the Timing menu, every channel is shown as a waveform.

Three predefined Timing Format Definition overlay files, part of the Futurebus+ bus support, are available for you to use when displaying data in the Timing menu. The files are installed on the DAS 9200 with the disassembler software. Table 5-1 shows which timing format file you can use for each support type and supplied setup.

Table 5-1
Supplied Timing Format Definition Files and Uses

Timing Format File Name	For Use With Support Type/ Supplied Setup
Fbus+_96	Fbus+ support FBus64 support
Fbus+Arb_96	FB_3-96 setup FB_2-96 setup
FB_Arb_96	FB_1-96 setup

The Fbus+_96 timing format file places the D127-96, D95-64, BP15-8, AD63-32, AD31-0, BP7-0, TG, CM, CA, ST, and Ph channel groups first and displays them as bus forms containing bus values instead of as individual timing waveforms. These groups are followed by the module clocking signal (generated by the probe adapter) and backplane handshake signals.

Figure 5-1 shows data displayed using the Fbus+_96 format file; the S1 switch is set to Async and clocking is Internal.

To select a supplied Timing Format Definition file, follow these steps:

1. Select the Timing menu and press F5: DEFINE FORMAT.
2. Press F5: RESTORE FORMAT.
3. Select Fbus+_96, Fbus+Arb_96, or FB_Arb_96 and press the Return key. A message tells you the format file is selected.
4. Press F8: EXIT & SAVE to return to the Timing menu.

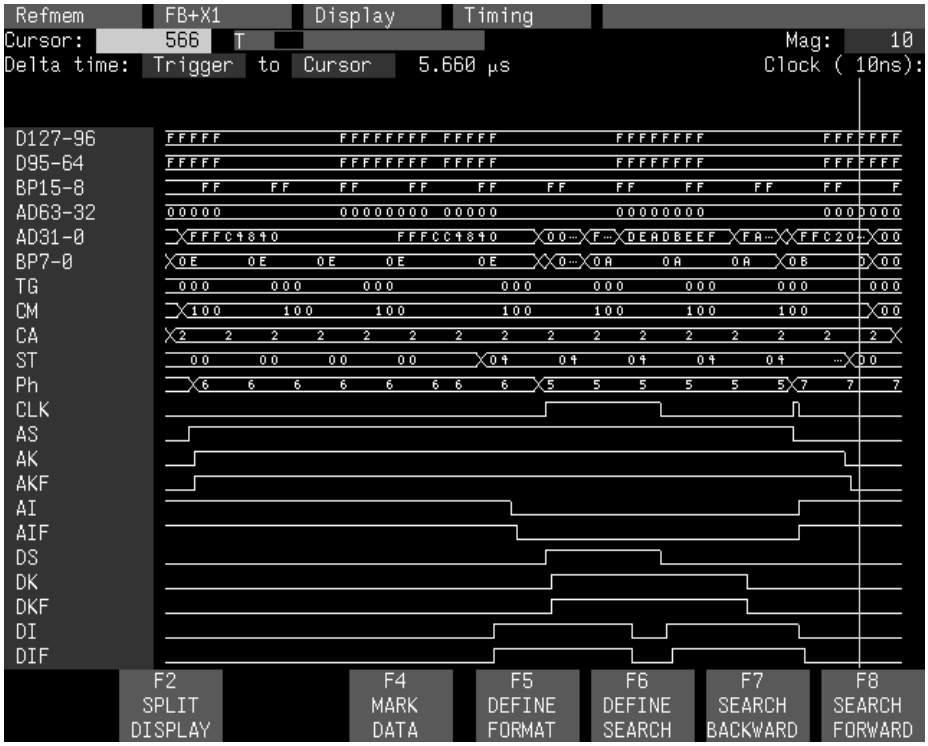


Figure 5-1. Timing data displayed using the Fbus+_96 timing format file.

State Menu

In the State menu, all channel group values are shown based on the selected radix in the Channel menu or the State Format Definition overlay. No disassembly of beat information (display or translation of acquired data) occurs.

Figure 5-2 shows State data; this is the same acquired data as shown in Figure 5-1.

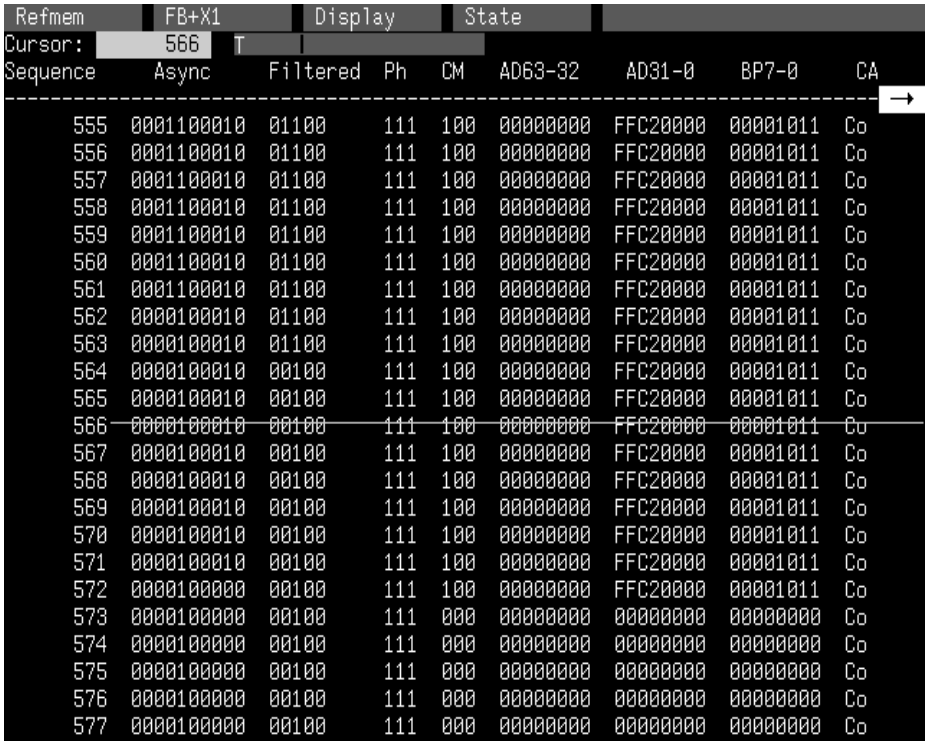


Figure 5-2. State data.

SEARCHING THROUGH DATA

To search through data, you can use either the Timing Search Definition overlay or the State Search Definition overlay. You can use these overlays and search through data as described in your *92A96 Module User Manual*.

PRINTING DATA

To print state data, you can use the State Print overlay. To access this overlay, press the Shift and Print keys at the same time from the State menu.

To print timing data, you can use the Timing Print overlay. To access this overlay, press the Shift and Print keys at the same time from the Timing menu.

For detailed information on the State Print overlay or the Timing Print overlay, refer to your *92A96 Module User Manual*.

Appendix A: ERROR MESSAGES AND DISASSEMBLY PROBLEMS

This appendix describes error messages and disassembly problems that you may encounter while acquiring data.

MODULE ERROR MESSAGES

These error messages will appear in the Module Monitor menu when there are problems with acquiring data or satisfying the trigger program. The error messages are listed in alphabetical order; a description of the error message and the recommended solution follow the error message.

Slow Clock. This message appears when the active clock channel (or channels) is not changing or is typically changing at 1 ms or slower intervals or one of the clock qualifiers is held in the wrong state. Check for the following:

- The Futurebus+ system is powered on and running. Make sure there is Futurebus+ bus activity.
- A supplied setup is restored in the Save/Restore menu, or that the Fbus64 or Fbus+ support is selected in the appropriate 92A96 Configuration menu.
- Custom is selected in the Clock menu for the Main bus.
- The connections between the 92A96 Module and the probe adapter are correct.

  The clock and 8-channel probe connections between the interface housings and probe adapter are correct (module name, clock, section names, and channel numbers match), are properly oriented (GND connects to ground), and are fully engaged.

  The connections between the interface housings and 92A96 probe cables have matched color labels, matched slot numbers, and are properly keyed.

  The connections between the 92A96 probe cables and probe connectors have matched color labels, matched slot numbers, and are properly keyed.

Waiting for Stop. This message appears when the trigger condition is satisfied and memory is full but the Manual Stop mode is selected in the Cluster Setup menu. The solution is to manually stop the DAS 9200 by pressing F1: STOP.

This message can also appear when other modules in the cluster have not filled their memories. Wait for the other modules to fill their memories. If the message does not disappear in a short time, press F1: STOP.

Waiting for Stop-Store. This message appears when the trigger condition is satisfied but the amount of post-fill memory specified in the trigger position field is not yet filled. Press F1: STOP to view the acquired data, then check for the following:

- The trigger program in the Trigger menu is correct.
- The storage qualification in the Trigger menu is correct.
- The Futurebus+ system activity has not stopped.

Waiting for Trigger. This message appears when the trigger condition doesn’t occur. Check for the following:

- The Futurebus+ system is powered on and running. Make sure there is Futurebus+ bus activity.
- The trigger conditions are not being satisfied. The Module Monitor menu shows which state events are not occurring. Press F1: STOP, access the Trigger menu, and redefine the conditions for that state. Also refer to the description on *Triggering* in Section 3.

OTHER DISASSEMBLY PROBLEMS

There may be problems with disassembly for which no error messages are displayed. Some of these problems and their recommended solutions follow.

Incorrect Data. If the data acquired is obviously incorrect, check the following:

- A supplied setup is restored in the Save/Restore menu, or that the Fbus64 or Fbus+ support is selected in the appropriate 92A96 Configuration menu.
- The connections between the 92A96 Modules and the probe adapter are correct.

  The clock and 8-channel probe connections between the interface housings and probe adapter are correct (module name, clock, section names, and channel numbers match), are properly oriented (GND connects to ground), and are fully engaged.

  The connections between the interface housings and 92A96 probe cables have matched color labels, matched slot numbers, and are properly keyed.

  The connections between the 92A96 probe cables and probe connectors have matched color labels, matched slot numbers, and are properly keyed.

- A constant timestamp delay (such as 10 ns) which indicates that the Sync/Async switch was set incorrectly for disassembly.

Other Suggestions. If the previous suggestions do not fix the problem with acquiring and disassembling Futurebus+ data, try restoring the DAS 9200 to a known state. You can do this by either restoring one of the supplied setup files from the Save/Restore menu, or by reloading the module setup by selecting Fbus64 or Fbus+ support in the 92A96 Configuration menu.

If the DAS 9200 still is not acquiring data after trying these solutions, there may be a problem with your Futurebus+ system. Try performing asynchronous timing acquisition with your DAS 9200 system to ensure that the Futurebus+ signals are valid at the time the probe adapter samples them.

Refer to *Section 5: General Purpose Analysis* for information on data sampling rates using either the Internal or External clocking selections in the Clock menu. Also refer to *Appendix B: How Data is Acquired* to see when the disassembler samples the various Futurebus+ system signals.

Appendix B: HOW DATA IS ACQUIRED

This appendix provides detailed information on how data is acquired and provides more information on signals acquired for disassembly as well as signals not acquired.

CLOCKING FOR THE MAIN BUS

Custom clocking used with the Main bus of the Futurebus+ system uses two sample points. After being logged in, these samples are sent to the trigger machine and the acquisition memory as a master sample (one complete data acquisition record). Refer to the *92A96 Module User Manual* for information on the trigger machine and master sample.

Figure B-1 shows when data is acquired from the Main bus. Signals shown are Main bus signals except for the DAS_CLK and LCONN_Y1-0 signals which are output by circuitry on the probe adapter.

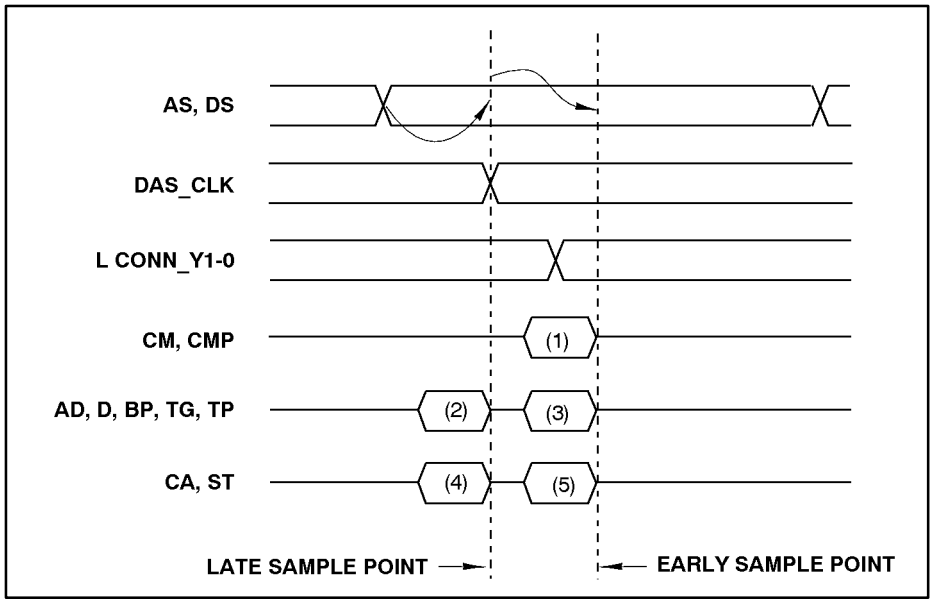


Figure B-1. Futurebus+ bus timing for the Main bus. The 92DM911 samples signals at the points shown above.

Logic on the probe adapter responds to rising and falling edges of AS and DS handshake lines (only). This can cause possible data capture at points (2) or (4), possible toggle of the DAS_CLK, possible change to the LCONN_Y1-0 signals at point (1), and possible acquisition of information at points (3) or (5).

The DAS 9200 responds to both the rising and falling edges of the DAS_CLK signal. No DAS_CLK edge is generated following the leading edge of AS.

The LCONN_Y1-0 signals indicate the beat type and show a disconnect beat (value of 11) initially. Their value for a connect beat is 10, for a first data beat of a partial is 00, and for other data beats is 01.

Capture of the AD, D, BP, TG, and TP signals can occur at either point (2) or (3). Capture depends on whether the information is available late in the previous beat (2) or early in the next beat (3). Connect beats, first data beats of partial reads, write data beats, and write disconnect beats are sampled at point (3). Normal read data beats, partial read data beats beyond the first data beat, and read disconnect beats are sampled at point (2).

During connect beats, data is not acquired at points (2) or (4).

During connect beats, ST0 is acquired at point (5), rather than at point (4) in the following beat, as usual. All other ST signals, and the CA signals are acquired at point (4).

Data acquired at points (1), (3), and (5) is retained by the logic on the probe adapter for recording in the DAS 9200 when the following edge of DAS_CLK occurs.

After DAS_CLK edge generation in response to the trailing edge of AS, the probe adapter logic cycles again to generate the final DAS_CLK edge to store the captured disconnect information.

Information acquired at sample point 2 and 4 at the final DAS_CLK edge is superfluous.

Under FBus+ or FBus64 support with Custom clocking set to not acquire power-up cycles, DAS_CLK edges occurring with POWERED0 (or POWERED1) off are ignored by the DAS 9200.

Custom Clocking

The Custom clocking algorithm has two variations: Power Up Cycles Acquired and Power Up Cycles Not Acquired.

Power Up Cycles Not Acquired. Power-up cycles are not logged in.

Power Up Cycles Acquired. Power-up cycles are logged in.

CLOCKING FOR THE ARB BUS

Figure B-2 shows when data is acquired from the Arb bus. Signals shown are Arb bus signals except for the AB_CLK which is output by the Arb bus circuitry on the probe adapter.

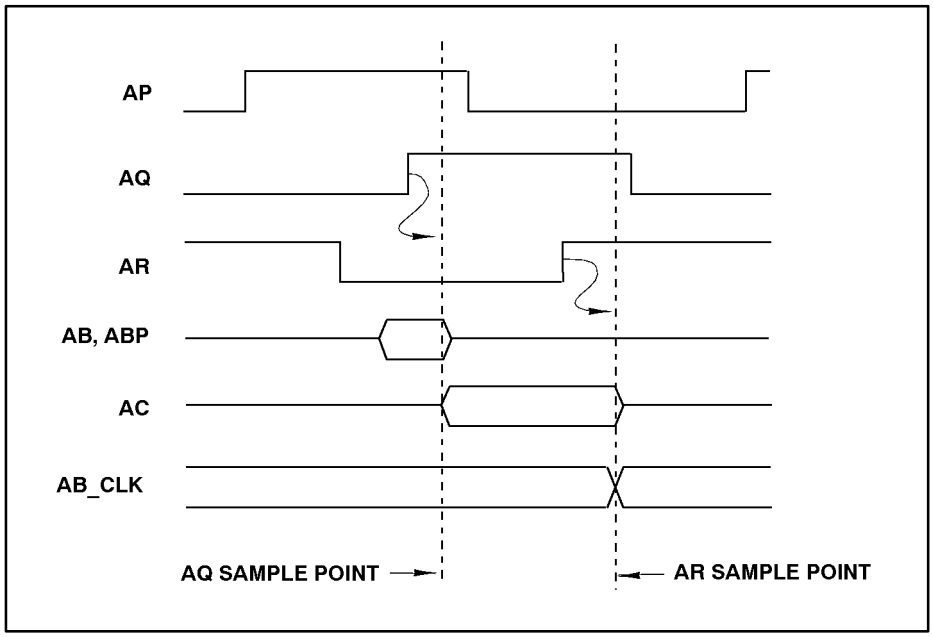


Figure B-2. Futurebus+ bus timing for the Arb bus.

Probe adapter logic responds to the leading edge of AQ by capturing AB and ABP information. Latch circuitry for AC capture is reset to 00.

Circuitry to capture AC information is always active, latching in 1s when AC1 or AC0 are asserted, and not changing when the bus signals are not asserted.

Probe adapter logic responds to the trailing edge of AR by toggling AB_CLK, resulting in captured AB, ABP, and AC information being recorded by the DAS 9200.

The DAS 9200 responds to both rising and falling edges of AB_CLK.

Under general purpose support with External clocking and the supplied clocking equation, AB_CLK edges occurring with POWERED off are ignored by the DAS 9200.

WARNING

The following servicing instructions are for use only by qualified personnel. To avoid personal injury, do not perform any servicing other than that contained in the operating instructions unless you are qualified to do so. Refer to the General Safety Summary and the Service Safety Summary prior to performing any service.

Appendix C: SERVICE INFORMATION

This appendix contains the following information:

- safety summary
- brief description of the probe adapter and how it works
- care and maintenance procedures
- specification tables
- channel assignment tables
- dimensions of the probe adapter
- removing and replacing individual signal leads
- removing and replacing sockets

SERVICE SAFETY INFORMATION

The following service safety information is for service technicians. Follow these safety precautions, along with the general precautions outlined in your *92A96 Module User Manual*, while installing or servicing this product.

Do Not Service Alone. Do not perform internal service or adjustment on this product unless another person is present and able to give first aid and resuscitation.

Use Care When Servicing With Power On. To avoid personal injury from dangerous voltages, remove jewelry such as rings, watches, and other metallic objects before servicing. Do not touch the product's exposed connections and components while power is on.

When plugged normally into a Futurebus+ system card cage, no low impedance power connections (except for ground) are exposed on the probe adapter.

PROBE ADAPTER DESCRIPTION

The probe adapter is a non-intrusive piece of hardware that allows the 92A96 Module to acquire data from an Futurebus+ bus in its own operating environment with essentially no effect on that system. Refer to Figure C-1 while reading the following discussion.

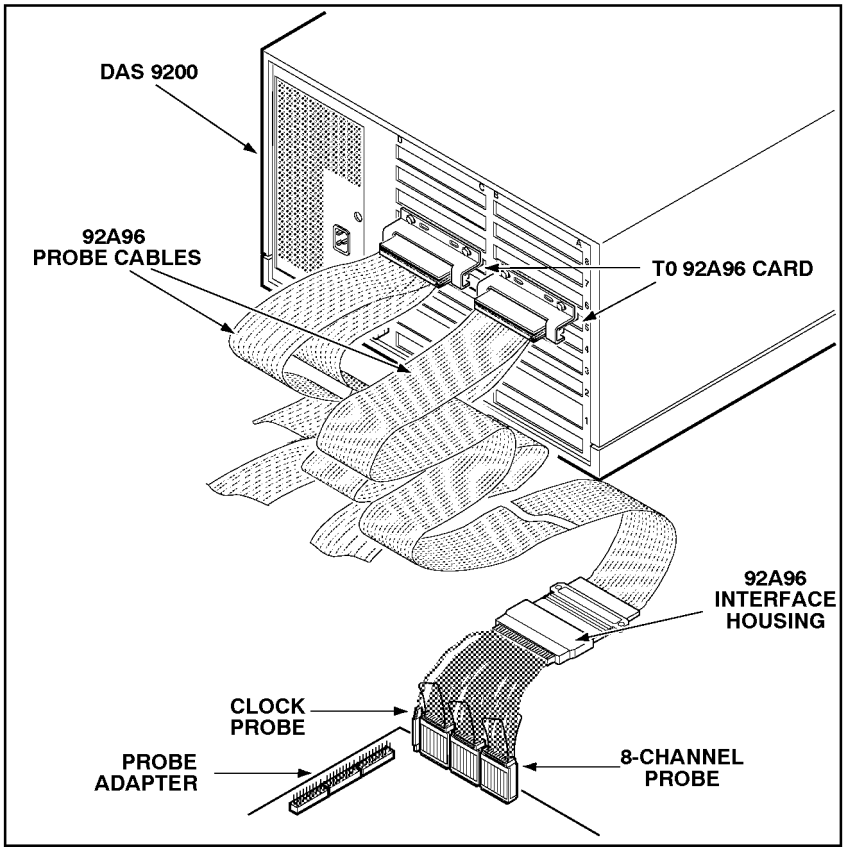


Figure C-1. Overview of the DAS 9200 connected to a typical probe adapter.

The probe adapter is a circuit board that installs into a Futurebus+ card cage and connects into the Futurebus+ backplane. Signals from the Futurebus+ system flow from the probe adapter to the podlet groups. The signals flow through the 92A96 probe cables to the 92A96 Modules. All circuitry on the probe adapter is powered from the Futurebus+ system under test.

CONFIGURING THE PROBE ADAPTER

There are two slide switches and two rotary switches on the probe adapter. The two slide switches are used to configure the probe adapter to acquire data from the Main or Arb buses for either synchronous (disassembly) or asynchronous (timing analysis) operation. One of the rotary switches is set to match the data path width of the Futurebus+ system backplane. The other rotary switch sets the glitch filter delay on the probe adapter.

Sync/Async Switches

The Sync/Async switches (S1 and S2) should be placed in the Sync position to acquire disassembly data, and in the Async position to acquire timing data. Use S1 to set probe adapter operation for the Main bus and S2 to set probe adapter operation for the Arb bus. Table 2-2 shows how to position these switches depending on the type of clocking you're using and the type of display you want to view.

Table C-1
Sync/Async Switches Information

Switch Positions	Clocking	Display Menu
S1, Main bus		
Sync (Disassembly)	Custom	Disassembly, Timing, or State
	Internal*	Timing or State
Async (Timing)	Internal	Timing or State
S2, Arb bus		
Sync (Disassembly)†	External	Disassembly†, Timing or State
	Internal*	Timing or State
Async (Timing)	Internal	Timing or State

*This choice is only useful for verifying probe adapter operation.
†Display of Arb bus data with Main bus disassembly requires correlating of the Arb bus module with the Main bus module.

Figure C-2 shows the locations of S1 and S2 on the probe adapter.

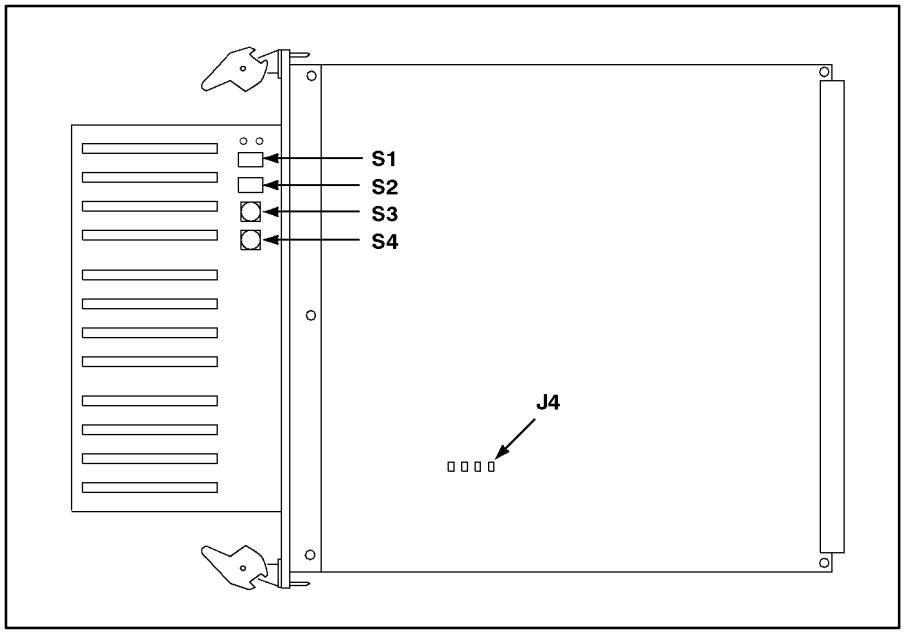


Figure C-2. Switch locations on the probe adapter.

In Sync (disassembly) operation, the probe adapter logic captures Futurebus+ data in bus transceiver devices for temporary storage until all information for the bus beat has been recorded by the 92A96 Module(s) in the DAS 9200.

In Async (timing) operation, the bus transceiver devices do not store any data. The signals from the Futurebus+ pass immediately through the probe adapter to the 92A96 Module(s) where their timing behavior is recorded.

Glitch Filter Delay Switch

The Glitch Filter Delay switch, S3, can be set to an appropriate setting to match the characteristics of your Futurebus+ system backplane. Table 2-3 shows how to position this switch.

Table C-2
Glitch Filter Delay Switch Positions

Switch Position	Nominal Delay*
0	13 ns
1	20 ns
2	27 ns
3	35 ns
*Twice the one-way backplane propagation delay.	

Figure C-2 shows the location of S3 on the probe adapter.

The probe adapter glitch filter circuitry makes filtered versions of eight Futurebus+ control signals available when timing analysis is performed. These Futurebus+ control signals are AR*, AI*, DK*, DI*, AP*, AQ*, AR*, and RE*. The filtered versions of these signals on the probe adapter are ARF, AIF, DKF, DIF, APF, AQF, and REF. Refer to Tables C-15 and C-17 for channel assignments of these signals.

Neither the position of S3 nor circuitry for the glitch filtering affect the acquisition of Main bus or Arb bus data by the probe adapter. (The Main bus logic uses the edges of only AS* and DS* to monitor the bus; the Arb bus logic uses only the falling (assertion) edges of AP*, AQ*, and AR*.)

Data Path Width Switch

Set the Data Path Width switch, S4, to match the width of the data bus portion of the Futurebus+ system backplane to which the probe adapter connects. Switch positions are for 32-, 64-, and 128-bit wide data buses.

Figure C-2 shows the location of S4 on the probe adapter.

The Data Path Width switch controls the operation of probe adapter bus transceiver devices associated with the Futurebus+ signals AD32* through AD63* (and parity signals BP4* through BP7*), and signals D64* through D127* (and parity signals BP8* through BP15*). This switch causes the transceivers for which no backplane signals exist to drive out low levels so that the transceiver's bus pins will not float electrically.

For example, with the switch set to a 128-bit wide data bus, all transceivers operate normally. With the switch set to a 64-bit wide data bus, transceiver pins for the D64* through D127* signals (and parity signals BP8* through BP15*) are held low.

It is important to set the Data Path Width switch correctly to avoid interfering with the operation of the Futurebus+ data bus.

Jumpers

Three jumpers, J1, J2, and J3, on the probe adapter should always be left open (no jumper). You cannot change the position of these jumpers and expect normal operation.

The last jumper, J4, controls whether live-insertion filtering is used in the acquisition of the AS* and DS* signals of the Main bus. These signals control the operation of the Main bus circuitry on the probe adapter. When J4 is not connected, filtering does not occur. When J4 is connected, filtering does occur.

Typically, J4 will not be connected unless you are using the probe adapter in a Futurebus+ system in which boards are installed and removed while the system is powered on. If you install or remove boards in your Futurebus+ system with power applied, then place a jumper on J4.

The presence of a jumper on J4 may negatively impact the ability of the probe adapter logic to properly acquire bus data in certain situations involving modules executing extremely high-speed handshakes. Therefore, J4 should be removed unless actually required.

NOTE

*Live insertion of the probe adapter is **not** supported. To avoid damage to the probe adapter and Futurebus+ system, plug the probe adapter into the backplane when the Futurebus+ system is powered off.*

NOTE

Do not install or remove J4 while the probe adapter is connected to a Futurebus+ system that is powered on; doing so may cause the Main bus circuitry on the probe adapter to enter an improper state.

If you change the jumper when the Futurebus+ system is powered on, you may have to reset the probe adapter circuitry.

There are two ways to reset the probe adapter. You can either power the Futurebus+ system off and then on, or you can momentarily short the POWERED signal of the probe adapter to ground. Table C-16 shows the channel assignment of the POWERED signal.

LED INDICATORS

There are two LEDs on the probe adapter. One lights when power is applied to the probe adapter, and the other lights when there is activity on the Futurebus+ bus.

The Power LED is red when the probe adapter is powered on. The Bus LED is yellow when either the AK* signal on the Main bus or the AP* signal on the Arb bus is asserted.

Figure C-3 shows the location of these LEDs on the probe adapter.

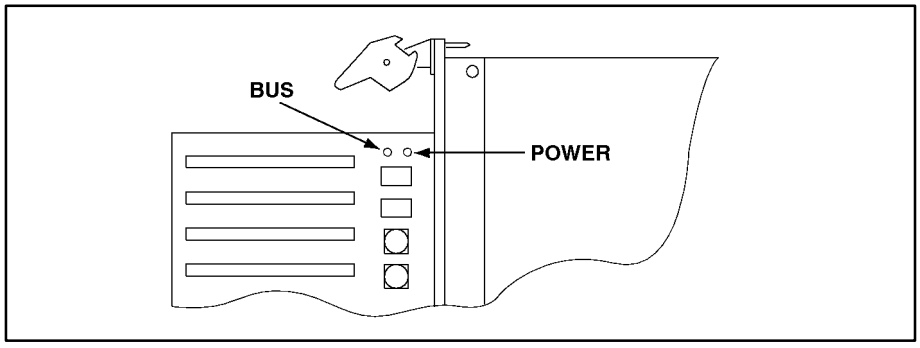


Figure C-3. LED locations on the probe adapter.

CARE AND MAINTENANCE

The probe adapter does not require scheduled or periodic maintenance. To maintain good electrical contact, keep the probe adapter free of dirt, dust, and contaminants. Also, ensure that any electrically conductive contaminants are removed.

Dirt and dust can usually be removed with a soft brush. For more extensive cleaning, use only a damp cloth. Abrasive cleaners and organic solvents should never be used.

CAUTION

The semiconductor devices contained on the probe adapter are susceptible to static-discharge damage. To prevent damage, service the probe adapter only in a static-free environment.

If the probe adapter is connected to your system, grasp the ground lug on the back of the PRISM mainframe to discharge your stored static electricity. If the probe adapter is not connected, touch any of the ground pins (row of square pins closest to the edge of the probe adapter circuit board labeled GND) to discharge stored static electricity from the probe adapter.

Always wear a grounding wrist strap, or similar device, while servicing the instrument.

Exercise care when soldering on a multilayer circuit board. Excessive heat can damage the through-hole plating or lift a run or pad and damage the board beyond repair. Do not apply heat for longer than three seconds. Do not apply heat consecutively to adjacent leads. Allow a moment for the board to cool between each operation.

If you must replace an electrical component on a circuit board, exercise extreme caution while unsoldering or soldering the new component. Use a pencil-type soldering iron of less than 18 watts and an approved unsoldering tool. Ensure that the replacement is an equivalent part by comparing the description as listed in the replaceable parts list.

CHANNEL ASSIGNMENTS

References to the LO and HI modules in the following tables apply to the variable-width module used to acquire 128-bit wide Main bus data. If you are acquiring 32- or 64-bit wide Main bus data, then only references to the LO module will apply to your setup.

Table C-3 shows the 92A96 section and channel assignments for the Ph (Phase) group starting with the most significant bit (MSB).

Table C-3
92DM911 Ph Group Channel Assignments

Bit Order	Module Section & Channel		Signal Name
	LO or HI	Sect : Chan	
MSB	LO	C2:1	POWERED0†
	LO	C2:7	LConn_Y1†
LSB	LO	C2:6	LConn_Y0†
†Signal generated by the probe adapter and not present on the Futurebus+ backplane.			

POWERED0 is a slowly-rising monotonic signal. When it is high, it indicates that the probe adapter logic has been initialized.

The LConn_Y1 and LConn_Y0 signals have a value of 10 for a connect beat, 00 for the first data beat of a partial transaction, 01 for any other data beat, and 11 for a disconnect beat.

Table C-4 shows the 92A96 section and channel assignments for the CM (Command) group starting with the most significant bit (MSB).

Table C-4
92DM911 CM Group Channel Assignments

Bit Order	Module Section & Channel		Signal Name
	LO or Hi	Sect : Chan	
MSB	LO	C2:2	CP
	LO	C0:7	CM_7
	LO	C0:6	CM_6
	LO	C0:5	CM_5
	LO	C0:4	CM_4†
	LO	C0:3	CM_3†
	LO	C0:2	CM_2†
	LO	C0:1	CM_1†
LSB	LO	C0:0	CM_0†
†Futurebus+ signal that controls or affects probe adapter logic operation.			

Table C-6 shows the 92A96 section and channel assignments for the AD63-32 group starting with the most significant bit (MSB).

Table C-5
92DM911 AD63-32 Group Channel Assignments

Bit Order	Module Section & Channel		Signal Name
	LO or HI	Sect : Chan	
MSB	LO	A3:7	AD_63
	LO	A3:6	AD_62
	LO	A3:5	AD_61
	LO	A3:4	AD_60
	LO	A3:3	AD_59
	LO	A3:2	AD_58
	LO	A3:1	AD_57
	LO	A3:0	AD_56
	LO	A2:7	AD_55
	LO	A2:6	AD_54
	LO	A2:5	AD_53
	LO	A2:4	AD_52
	LO	A2:3	AD_51
	LO	A2:2	AD_50
	LO	A2:1	AD_49
	LO	A2:0	AD_48
	LO	A1:7	AD_47
	LO	A1:6	AD_46
	LO	A1:5	AD–45
	LO	A1:4	AD_44
	LO	A1:3	AD_43
	LO	A1:2	AD_42
	LO	A1:1	AD_41
	LO	A1:0	AD_40
	LO	A0:7	AD_39
	LO	A0:6	AD_38
	LO	A0:5	AD_37
	LO	A0:4	AD_36
	LO	A0:3	AD_35
	LO	A0:2	AD_34
	LO	A0:1	AD_33
LSB	LO	A0:0	AD_32

Table C-6 shows the 92A96 section and channel assignments for the AD31-0 group starting with most significant bit (MSB).

Table C-6
92DM911 AD31-0 Group Channel Assignments

Bit Order	Module Section & Channel		Signal Name
	LO or HI	Sect : Chan	
MSB	LO	D3:7	AD_31
	LO	D3:6	AD_30
	LO	D3:5	AD_29
	LO	D3:4	AD_28
	LO	D3:3	AD_27
	LO	D3:2	AD_26
	LO	D3:1	AD_25
	LO	D3:0	AD_24
	LO	D2:7	AD_23
	LO	D2:6	AD_22
	LO	D2:5	AD_21
	LO	D2:4	AD_20
	LO	D2:3	AD_19
	LO	D2:2	AD_18
	LO	D2:1	AD_17
	LO	D2:0	AD_16
	LO	D1:7	AD_15
	LO	D1:6	AD_14
	LO	D1:5	AD_13
	LO	D1:4	AD_12
	LO	D1:3	AD_11
	LO	D1:2	AD_10
	LO	D1:1	AD_9
	LO	D1:0	AD_8
	LO	D0:7	AD_7
	LO	D0:6	AD_6
	LO	D0:5	AD_5
	LO	D0:4	AD_4
	LO	D0:3	AD_3
	LO	D0:2	AD_2
	LO	D0:1	AD_1
LSB	LO	D0:0	AD_0

Table C-7 shows the 92A96 section and channel assignments for the BP7-0 group starting with the most significant bit (MSB).

Table C-7
92DM911 BP7-0 Group Channel Assignments

Bit Order	Module Section & Channel		Signal Name
	LO or HI	Sect : Chan	
MSB	LO	C1:7	BP_7
	LO	C1:6	BP_6
	LO	C1:5	BP_5
	LO	C1:4	BP_4
	LO	C1:3	BP_3
	LO	C1:2	BP_2
	LO	C1:1	BP_1
LSB	LO	C1:0	BP_0

Table C-8 shows the 92A96 section and channel assignments for the CA (Capability) group starting with the most significant bit (MSB).

Table C-8
92DM911 CA Group Channel Assignments

Bit Order	Module Section & Channel		Signal Name
	LO or Hi	Sect : Chan	
MSB	LO	C2:5	CA_2
	LO	C2:4	CA_1†
LSB	LO	C2:3	CA_0
†Futurebus+ signal that controls or affects probe adapter logic operation.			

Table C-9 shows the 92A96 section and channel assignments for the ST (Status) group starting with the most significant bit (MSB).

Table C-9
92DM911 ST Group Channel Assignments

Bit Order	Module Section & Channel		Signal Name
	LO or HI	Sect : Chan	
MSB	LO	C3:7	ST_7
	LO	C3:6	ST_6
	LO	C3:5	ST_5
	LO	C3:4	ST_4
	LO	C3:3	ST_3
	LO	C3:2	ST_2
	LO	C3:1	ST_1
LSB	LO	C3:0	ST_0†
†The ST_0 signal has additional latching logic in its data path on the probe adapter which may cause its propagation delay in Async operation to be somewhat greater than other signals. In Sync operation, this latching logic may also cause changes in ST_0 in beats other than connect beats to apparently log behind the other ST signals.			

Table C-10 shows the 92A96 section and channel assignments for the D127-96 group starting with most significant bit (MSB).

Table C-10
92DM911 D127-96 Group Channel Assignments

Bit Order	Module Section & Channel		Signal Name
	LO or HI	Sect : Chan	
MSB	HI	A3:7	D_127
	HI	A3:6	D_126
	HI	A3:5	D_125
	HI	A3:4	D_124
	HI	A3:3	D_123
	HI	A3:2	D_122
	HI	A3:1	D_121
	HI	A3:0	D_120
	HI	A2:7	D_119
	HI	A2:6	D_118
	HI	A2:5	D_117
	HI	A2:4	D_116
	HI	A2:3	D_115
	HI	A2:2	D_114
	HI	A2:1	D_113
	HI	A2:0	D_112
	HI	A1:7	D_111
	HI	A1:6	D_110
	HI	A1:5	D_109
	HI	A1:4	D_108
	HI	A1:3	D_107
	HI	A1:2	D_106
	HI	A1:1	D_105
	HI	A1:0	D_104
	HI	A0:7	D_103
	HI	A0:6	D_102
	HI	A0:5	D_101
	HI	A0:4	D_100
	HI	A0:3	D_99
	HI	A0:2	D_98
	HI	A0:1	D_97
LSB	HI	A0:0	D_96

Table C-10 shows the 92A96 section and channel assignments for the D95-64 group starting with most significant bit (MSB).

Table C-11
92DM911 D95-64 Group Channel Assignments

Bit Order	Module Section & Channel		Signal Name
	LO or HI	Sect : Chan	
MSB	HI	D3:7	D_95
	HI	D3:6	D_94
	HI	D3:5	D_93
	HI	D3:4	D_92
	HI	D3:3	D_91
	HI	D3:2	D_90
	HI	D3:1	D_89
	HI	D3:0	D_88
	HI	D2:7	D_87
	HI	D2:6	D_86
	HI	D2:5	D_85
	HI	D2:4	D_84
	HI	D2:3	D_83
	HI	D2:2	D_82
	HI	D2:1	D_81
	HI	D2:0	D_80
	HI	D1:7	D_79
	HI	D1:6	D_78
	HI	D1:5	D_77
	HI	D1:4	D_76
	HI	D1:3	D_75
	HI	D1:2	D_74
	HI	D1:1	D_73
	HI	D1:0	D_72
	HI	D0:7	D_71
	HI	D0:6	D_70
	HI	D0:5	D_69
	HI	D0:4	D_68
	HI	D0:3	D_67
	HI	D0:2	D_66
	HI	D0:1	D_65
LSB	HI	D0:0	D_64

Table C-12 shows the 92A96 section and channel assignments for the BP15-8 group starting with the most significant bit (MSB).

Table C-12
92DM911 BP15-8 Group Channel Assignments

Bit Order	Module Section & Channel		Signal Name
	LO or HI	Sect : Chan	
MSB	HI	C1:7	BP_15
	HI	C1:6	BP_14
	HI	C1:5	BP_13
	HI	C1:4	BP_12
	HI	C1:3	BP_11
	HI	C1:2	BP_10
	HI	C1:1	BP_9
LSB	HI	C1:0	BP_8

Table C-13 shows the 92A96 section and channel assignments for the TG (Tag) group starting with the most significant bit (MSB).

Table C-13
92DM911 TG Group Channel Assignments

Bit Order	Module Section & Channel		Signal Name
	LO or HI	Sect : Chan	
MSB	HI	C2:0	TP
	HI	C0:7	TG_7
	HI	C0:6	TG_6
	HI	C0:5	TG_5
	HI	C0:4	TG_4
	HI	C0:3	TG_3
	HI	C0:2	TG_2
	HI	C0:1	TG_1
LSB	HI	C0:0	TG_0

Table C-14 shows the 92A96 section and channel assignments for the Async (Asynchronous) group.

Table C-14
92DM911 Async Group Channel Assignments

Module Section & Channel		Signal Name
LO or HI	Sect : Chan	
LO	C2:0	CLK†
HI	C3:1	RE
HI	C3:7	AS‡
HI	C3:5	AK
HI	C3:6	AI
HI	C3:4	DS‡
HI	C3:2	DK
HI	C3:3	DI
HI	C3:0	ET
HI	C2:2	PE

†Signal generated by the probe adapter and not present on the Futurebus+ backplane.
‡Futurebus+ signal that controls or affects probe adapter logic operation.

The CLK signal is a replica of the module's clocking signal DAS_CLK.

Table C-15 shows the 92A96 section and channel assignments for the Filtered group.

Table C-15
92DM911 Filtered Group Channel Assignments

Module Section & Channel		Signal Name
LO or HI	Sect : Chan	
HI	C2:3	REF†
HI	C2:6	AKF†
HI	C2:7	AIF†
HI	C2:4	DKF†*
HI	C2:5	DIF†

†Signal generated by the probe adapter and not present on the Futurebus+ backplane.

The following four tables show channel assignments for the Arb bus module.

Table C-16 shows the 92A96 section and channel assignments for the ArbAsync (Arb Asynchronous) group.

Table C-16
92DM911 ArbAsync Group Channel Assignments

Sect : Chan	Signal Name
D3:7	AP†
D3:6	AQ†
D3:5	AR†
D3:4	ARB_CLK‡
C2:1	POWERED‡
C2:0	INIT_L‡

†Futurebus+ signal that controls or affects probe adapter logic operation.
‡Signal generated by the probe adapter and not present on the Futurebus+ backplane.

The ARB_CLK signal is a replica of the module's clocking signal AB_CLK. POWERED is a slowly-rising monotonic signal. When it is high, it indicates that the probe adapter logic has been initiated. The INIT_L signal is a fast-edged version of POWERED.

Table C-17 shows the 92A96 section and channel assignments for the ArbFiltd (Arb Filtered) group.

Table C-17
92DM911 ArbFiltd Group Channel Assignments

Sect : Chan	Signal Name
D3:2	APF†
D3:1	AQF†
D3:0	ARF†

†Signal generated by the probe adapter and not present on the Futurebus+ backplane.

Table C-18 shows the 92A96 section and channel assignments for the AC (Arb Condition) group starting with the most significant bit (MSB).

Table C-18
92DM911 AC Group Channel Assignments

Bit Order	Sect : Chan	Signal Name
MSB	D2:6	AC_1†
	D2:5	AC_0†

†The AC_0 and AC_1 signals have additional latching logic in their data path on the probe adapter which may cause their propagation delay in Async operation to be somewhat greater than other signals. In Sync operation, this latching logic may also cause changes in AC_0 and AC_1 in beats other than connect beats to apparently log behind other signals.

Table C-19 shows the 92A96 section and channel assignments for the AB group starting with the most significant bit (MSB).

Table C-19
92DM911 AB Group Channel Assignments

Bit Order	Sect : Chan	Signal Name
MSB	D2:7	ABP
	D0:7	AB_7
	D0:6	AB_6
	D0:5	AB_5
	D0:4	AB_4
	D0:3	AB_3
	D0:2	AB_2
	D0:1	AB_1
LSB	D0:0	AB_0

The 92A96 section and channel assignment for the S1 (Serial) group is D2:4 and the signal name is SB1. This signal is not logically part of either the Main bus or Arb bus.

The LO Main bus module acquires data with Custom clocking which uses both edges of LO_CLK0 qualified by the POWERED signal on LO_C2:1 if power-up cycles are not acquired.

The HI Main bus module acquires data with Custom clocking which uses both edges of HI_CLK0 qualified by the POWERED signal on HI_C2:1 if power-up cycles are not acquired.

The Arb bus module acquires data with External clocking which uses both edges of CLK0 qualified by the POWERED signal on C2:1 if power-up cycles are not acquired.

The 92DM911 does not provide access for all Futurebus+ backplane signals. These signals are: RQ1-0, GR, GA4-0 (capacitive bypass to ground provided), SB0, all reserved, and all I/O.

DISCONNECTING PROBES

You may need to disconnect the clock and 8-channel probes from the probe adapter to use them on another application, to connect individual podlets to other signals in your Futurebus+ system, or to replace defective clock or probe channels (podlets). Refer to Figure C-4 and the following procedure to disconnect the clock and 8-channel probes from the probe adapter. Use the antistatic shipping material to support the probe adapter while disconnecting the clock and 8-channel probes.

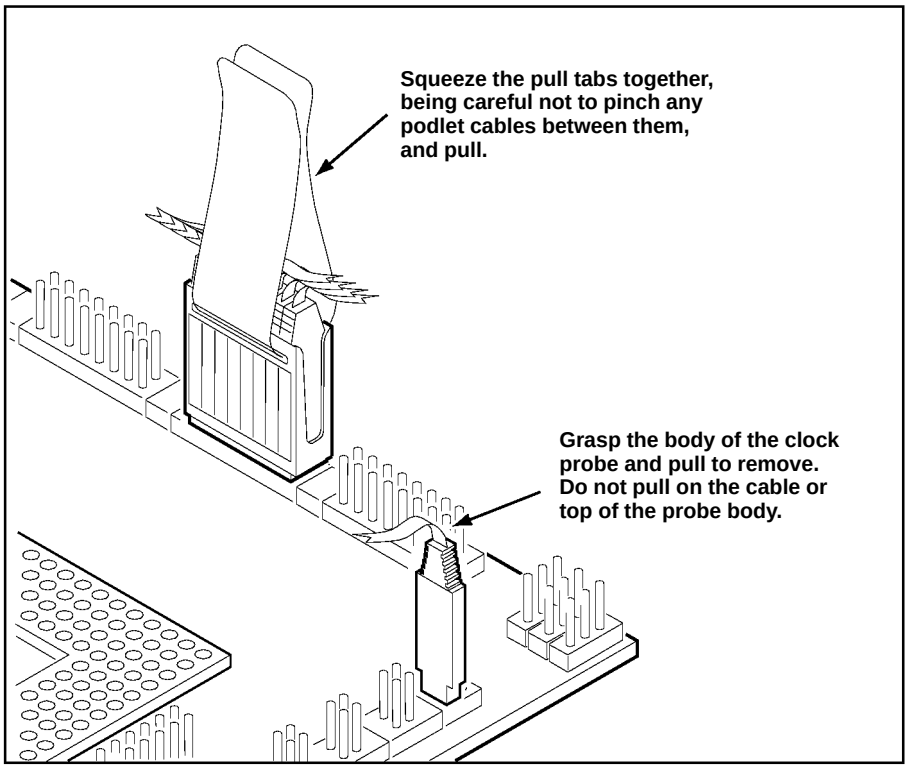


Figure C-4. Disconnecting clock and 8-channel probes.

1. Power down the SUT. It is not necessary to power down the DAS 9200.

CAUTION

Pulling on the cables, on the neck of an individual probe, or pinching the cables between the pull tabs can damage the probes. Always handle the probes by their bodies.

2. Firmly grasp the body of a clock probe and gently pull it off of the square pins.
3. Squeeze the pull tabs on the podlet holder together, be careful not to pinch any podlet cables between them.
4. Gently pull the 8-channel probe off of the square pins.

REMOVING AND REPLACING PODLETS

Each 8-channel probe consists of 8 single-channel podlets ganged together in a podlet holder. You may need to remove these podlets from the 8-channel probe to use for alternate connections to Futurebus+ system signals.

Refer to the discussions on *Signals* in Appendix A and *Alternate Connections* in Section 2 for information about which channels you can use to make alternate connections between the DAS 9200 and system under test without disturbing the channel connections required for disassembly.

You can also use these procedures to replace a defective clock probe or a defective podlet from an 8-channel probe.

Removing a Clock Probe or 8-Channel Probe Podlet from the Interface Housing

Refer to Figure C-5 and the following procedure to remove a clock probe or an 8-channel probe podlet from the interface housing.

1. Power down the SUT. It is not necessary to power down the DAS 9200.
2. Use a small pointed tool such as a ballpoint pen, pencil, or straightened paper clip to press down on the latch detent of the podlet through an opening on the interface housing.
3. Gently pull the podlet connector out of the housing with one hand while pressing down on the latch detent with the pointed tool.

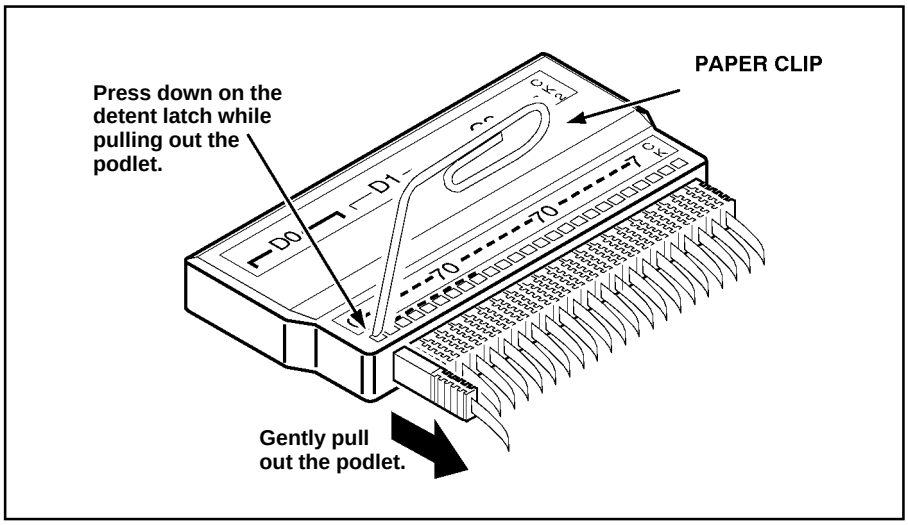


Figure C-5. Removing a probe podlet from the interface housing.

Replacing a Clock Probe

To replace a clock probe, insert a new clock probe into the same clock channel position on the interface housing. Insert the clock probe into the interface housing with the detent latch oriented to the label side of the housing. Refer to Figure C-5.

Removing 8-Channel Probe Podlets from the Podlet Holder

Refer to Figure C-6 and the following procedure to remove the 8-channel probe podlets from the podlet holder.

CAUTION

Excessive pulling on the sides of the holder can damage the podlet holder. Spread the holder open wide enough to clear and remove the podlets.

1. To remove podlets from the podlet holder, grasp the plastic pull tab on each side of the podlet holder and gently spread the sides of the holder open just enough to clear a podlet.
2. Remove the middle two podlets from the podlet holder by pushing up on the metal pin receptacles.
3. Release the tabs on the podlet holder.
4. Remove the remaining podlets by turning and extracting each one at a time.

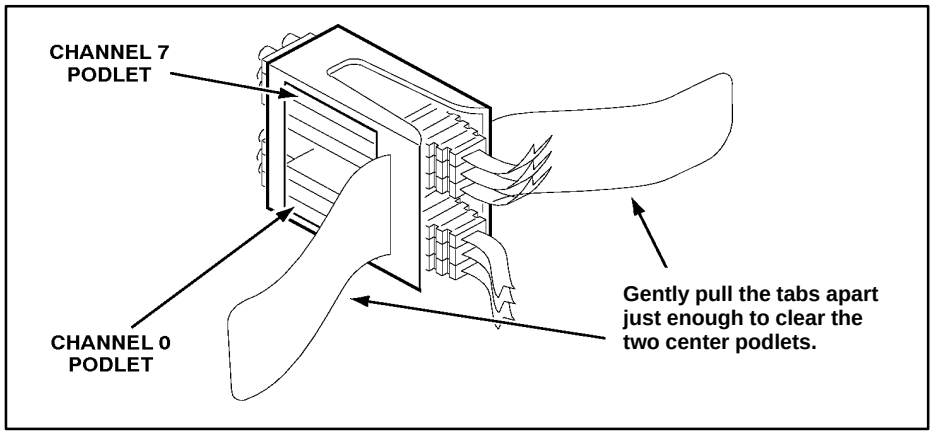


Figure C-6. Ganging together the 8-channel probe podlets.

Replacing 8-Channel Probe Podlets

The channel podlets must retain the same channel order on both the interface housing and in the podlet holder. Be sure to replace the old podlet with a podlet of the same color. Table C-20 shows the color code and channel number of each podlet for an 8-channel probe.

Table C-20
Podlet-to-Channel Color Code

Podlet Color	Channel
Black	0
Brown	1
Red	2
Orange	3
Yellow	4
Green	5
Blue	6
Violet	7

Refer to Figure C-6 and the following procedure to replace an 8-channel probe podlet.

1. Insert the appropriately-colored podlet into the interface housing with the detent latch oriented to the label side of the housing.
2. If you are replacing a single podlet, orient the podlet connector marked GND towards the side of the podlet holder labeled GROUND.
3. Grasp the plastic pull tab on each side of the holder and gently spread the sides of the holder open just enough to clear the podlet.

4. Hold the podlet body with the other hand and place it in the holder in the correct channel order. Do not grasp and turn the podlet cable.
5. If you are reganging all the podlets of an 8-channel probe, begin ganging the podlets together starting with either channel 0 or channel 7. Orient the podlet channel marked GND towards the side of the podlet holder labeled GROUND.

CAUTION

Avoid twisting the podlet cables between the interface housing and the podlet holder. To prevent damage to the podlets, keep the podlet cables parallel to each other when ganging them into the holder.

6. Hold the podlet body, turn the podlet body parallel to the sides of the holder, move it into the holder, and use your fingers to press it into place perpendicular to the sides of the holder. Be sure to gang the podlets in the correct channel order according to the channel label on the podlet holder and podlet color code, with all ground channels toward the Ground side of the holder. Do not place the podlet into the holder by grasping the podlet cable.
7. Continue placing the next two podlets, one at a time, in channel order, in the podlet holder. Orient all ground channels toward the Ground side of the holder.
8. The fourth podlet should be either channel 0 or 7, whichever one is not already placed in the holder. Place this podlet in the other end of the podlet holder and orient the ground channel correctly.
9. Continue placing the next two podlets, one at a time, in channel order, in the podlet holder. Continue orienting the ground channels correctly.

CAUTION

Excessive pulling on the sides can break the podlet holder. Spread the holder open only wide enough to clear the podlet.

10. Grasp the plastic pull tab on each side of the holder and gently spread the sides of the holder open just enough to clear a podlet.
11. Place the last pair of podlets (channels 3 and 4) in the podlet holder in proper channel order, orienting the ground channels to the Ground side of the holder.

REPLACEABLE PARTS LIST

This section contains a list of the components that are replaceable for the 92DM911 Probe Adapter. As described below, use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available from or through your local Tektronix, Inc. service center or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest circuit improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part Number
- Instrument Type or Model Number
- Instrument Serial Number
- Instrument Modification Number, if applicable

If a part you order has been replaced with a different or improved part, your local Tektronix service center or representative will contact you concerning any change in the part number.

Change information, if any, is located at the rear of this manual.

Module Replacement

The 92DM911 Probe Adapter is serviced by module replacement so there are three options you should consider:

Module Exchange — In some cases you may exchange your module for a remanufactured module. These modules cost significantly less than new modules and meet the same factory specifications. For more information about the module exchange program, call 1-800-TEKWIDE, extension BV 5799.

Module Repair — You may ship your module to us for repair, after which we will return it to you.

New Modules — You may purchase new replacement modules in the same way as other replacement parts.

Using the Replaceable Parts List

The tabular information in the Replaceable Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find the all the information you need for ordering replacement parts.

Item Names

In the Replaceable Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, U.S. Federal Cataloging Handbook H6-1 can be used where possible.

Indentation System

This parts list is indented to show the relationship between items. The following example is of the indentation system used in the Description column:

1 2 3 4 5 Name & Description

Assembly and/or Component
Attaching parts for Assembly and/or Component
(END ATTACHING PARTS)
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
(END ATTACHING PARTS)
Parts of Detail Part
Attaching parts for Parts of Detail Part
(END ATTACHING PARTS)

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. Attaching parts must be purchased separately, unless otherwise specified.

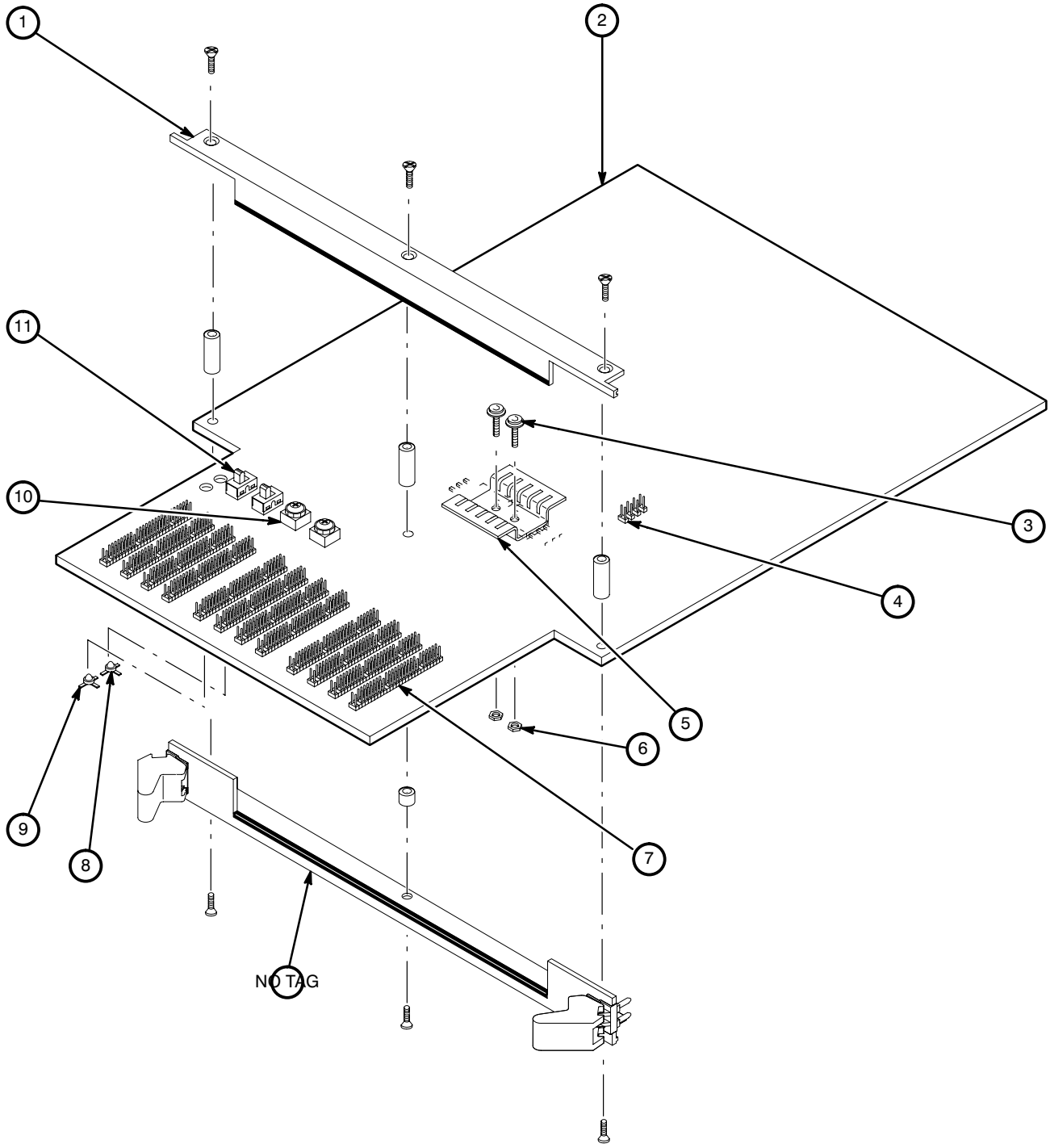
Abbreviations

Abbreviations conform to American National Standards Institute (ANSI) standard Y1.1.

CROSS INDEX – MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
TK0435	LEWIS SCREW CO	4300 S RACINE AVE	CHICAGO IL 60609−3320
04426	ITW SWITCHES DIV OF ILLINOIS TOOL WORKS INC	6615 W IRVING PARK RD	CHICAGO IL 60634−2410
13103	THERMALLOY CO INC	2021 W VALLEY VIEW LN PO BOX 810839	DALLAS TX 75381
50434	HEWLETT−PACKARD CO OPTOELECTRONICS DIV	370 W TRIMBLE RD	SAN JOSE CA 95131
57856	TELTEC INC	7890 12TH AVE SOUTH	MINNEAPOLIS MN 55425
58050	TEKA PRODUCTS INC	45 SALEM ST	PROVIDENCE RI 02907
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077−0001
93907	TEXTRON INC CAMCAR DIV	600 18TH AVE	ROCKFORD IL 61108−5181

Fig. & Index No.	Tektronix Part No.	Serial No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
1−0	010−0554−00			1	PROBE,ADAPTER:BUS PROBE ADAPTER	80009	010055400
−1	333−4026−00			1	PANEL,FRONT:92DM911 (INCLUDES ATTACH ING HARDWARE)	80009	333402600
−2	671−2529−00			1	CIRCUIT BD ASSY:FUTUREBUS + PROBE ADAPT	80009	671252900
−3	211−0409−00			2	SCR,ASSEM WSHR:4−40 X 0.312,PNH,STLTORX	93907	829−06888−024
−4	131−1857−00			1	CONN,HDR:PCB,;MALE,STR,1 X 36,0.1 CTR,0.23 (J1,J2,J3,& J4)	58050	082−3644−SS10
−5	214−2957−00			1	HEAT SINK,XSTR:TO−220,AL	13103	6072B
−6	210−0551−00			2	NUT,PLAIN,HEX:4−40 X 0.25,ST CD PL	TK0435	ORDER BY DESC
−7	131−5267−00			12	CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (J8,J9,J10,J11,J12,J13,J14,J15,J16,J17,J18 & J19)	80009	131526700
−8	150−5004−00			1	DIODE,OPTO:,LED;HI EFFIC RED,635NM,1.0 MCD (DS3202)	50434	HLMP6300−021
−9	150−5006−00			1	DIODE,OPTO:,LED;YEL,585NM,0.4MCD AT 2MA (DS3200)	50434	HLMP−7019−021
−10	260−2233−00			2	SWITCH,,ROTARY:REAL CODE,DIP (S1,S2)	57856	KDS 10−312
−11	260−1641−00			2	SWITCH,SLIDE:DPDT,0.5A,125 VAC (S3,S4)	04426	8524923−021−114
					STANDARD ACCESSORIES		
	070−8747−00			1	MANUAL,TECH:INSTR,92DM911,FUTUREBUS	80009	070874700
	061−3977−01			1	SUPPORT SHEET,TECHNICAL:92DM911	80009	061397700
	063−1224−00			1	FUTUREBUS + RELEASE NOTES SOFTWARE	80009	063122400



Exploded view.

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